

# Parameter Extraction for a Power Diode Circuit Simulator Model Including Temperature Dependent Effects

X. Kang, A. Caiafa, E. Santi, J.L. Hudgins, P.R. Palmer\*

Department of Electrical Engineering  
University of South Carolina  
Columbia, SC 29208, USA  
santi@enr.sc.edu

\*Department of Engineering  
University of Cambridge  
Trumpington Street  
Cambridge CB2 1PZ, UK

**Abstract** – Power electronics designers need accurate models of power diodes to perform simulations of the systems they are designing. The diode models should be accurate under a wide variety of operating conditions. In particular temperature dependencies should be accurately modeled. Physics-based models appear to be the best choice to meet these requirements. On the other hand, complicated parameter extraction procedures discourage use of these models by practicing engineers. In this work we explore the possibility of using a sophisticated physics-based diode model utilizing at most three parameters obtained directly or estimated from the manufacturer’s data sheets. In order to validate the proposed approach, several diodes with different characteristics are tested under different conditions and a wide temperature range from –150 to 150 °C. Experimental results are compared with simulations.\*

## I. INTRODUCTION

Power electronics designers need accurate models of power diodes to perform simulations of the systems they are designing. The diode models should be accurate under a wide variety of operating conditions. In particular temperature dependencies should be accurately modeled. Physics-based models appear to be the best choice to meet these requirements. On the other hand, complicated parameter extraction procedures discourage use of these models by practicing engineers. In this work we explore the possibility of using a sophisticated physics-based diode model requiring at most three parameters estimated from the manufacturer’s data sheets and refined with a simple turn-off test. The model is implemented in PSpice, but because of the equivalent circuit form of the model, it could easily be implemented in other circuit simulators such as Saber or in system simulators such as the Virtual Test Bed (VTB). In order to validate the proposed approach, several diodes with different characteristics are tested under different conditions and at different temperatures. The experimental results are compared with simulations.

The behavior of a pin diode is dominated by the drift region characteristics. The parameters needed for the diode model are the drift region width,  $W$ , the active die area,  $A$ , the effective high level lifetime,  $\tau$ , and the impurity doping density in the drift region,  $N_B$ . All of these parameters can be directly obtained or estimated from the data sheets. In particular, the drift region width can be estimated based on

the diode blocking voltage, the active die area can be estimated from the diode current rating, and the high level lifetime can be estimated from the reverse recovery time and reverse recovery charge specified in the data sheets. The background doping in the drift region  $N_B$  is usually in the range from  $6 \times 10^{13}$  to  $2 \times 10^{14}$  cm<sup>-3</sup> for high voltage diodes. All other parameters in the model are derived using these four parameters and other known semiconductor parameters, such as carrier mobility. The model also includes the parameters’ associated temperature dependencies.

## II. ELECTRO-THERMAL PHYSICS-BASED MODEL

### A. Background

The behavior of conductivity modulated devices, such as pin diodes and IGBTs, depends heavily on the excess carrier (charge) distribution in the wide drift region. In modern pin diodes, the charge profile has a 1D form over most of its volume [1]. Thus, a 1D solution is adequate for the bulk of the device. Space-charge neutrality is maintained with the majority carrier profile closely matching the minority carrier profile (quasi-neutrality). Under these conditions, and assuming high-level injection, the charge dynamics are described by the ambipolar diffusion equation (1):

$$D \frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{\tau} + \frac{\partial p(x,t)}{\partial t} \quad (1)$$

where  $D$  is the ambipolar diffusion coefficient,  $\tau$  is the high-level carrier lifetime within the drift region and  $p(x,t)$  is the excess carrier concentration. A Fourier based solution for this equation has been proposed [1]. The 2<sup>nd</sup> order partial differential carrier diffusion equation is converted into an infinite set of 1<sup>st</sup> order linear differential equations with series coefficients  $p_0 \dots p_k$  forming equivalent  $R_n C_n$  components.

$$p(x,t) = p_0(t) + \sum_{k=1}^{\infty} p_k(t) \cos \left[ \frac{k\pi(x-x_1)}{x_2-x_1} \right] \quad (2)$$

The representation requires the width of the undepleted region and the hole and electron currents at the boundaries of the region ( $x_1$  and  $x_2$ ), which give the gradients of the carrier concentrations,  $f(t)$  and  $g(t)$ , at  $x_1$  and  $x_2$ , respectively. The functions  $f(t)$  and  $g(t)$  are defined by (3) and (4) as follows:

$$f(t) = \left[ \frac{\partial p(x,t)}{\partial t} \right]_{x_1} = \frac{1}{2qA} \left[ \frac{I_{n_1}}{D_n} - \frac{I_{p_1}}{D_p} \right] \quad (3)$$

\*This work was supported by the U.S. Office of Naval Research under Grant N00014-00-1-0131.

$$g(t) = \left[ \frac{\partial p(x,t)}{\partial t} \right]_{x_2} = \frac{1}{2qA} \left[ \frac{I_{n_2}}{D_n} - \frac{I_{p_2}}{D_p} \right] \quad (4)$$

$A$  is the cross-sectional area of the device,  $D_n$  and  $D_p$ , the electron and hole diffusion coefficients,  $I_{n_1}$  and  $I_{p_1}$  the electron and hole currents at  $x = x_1$  (p side), and  $I_{n_2}$  and  $I_{p_2}$  the electron and hole currents at  $x = x_2$  (n side). A schematic of the n-drift region where the ambipolar diffusion equation is solved using boundary currents from (3) and (4) is shown in Fig.1. Clearly, the success of the approach now depends solely upon developing the boundary conditions.

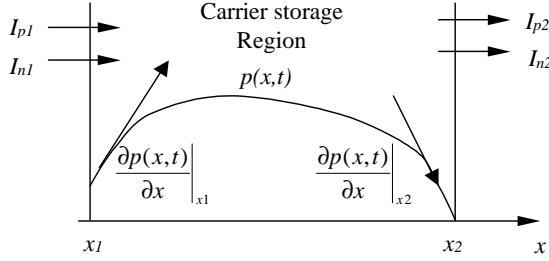


Fig. 1. Undepleted n-drift showing stored charge and boundary currents.

### B. Equivalent circuit modeling the distributed charge

The model developed is primarily concerned with accurately capturing the physical behavior of the stored charge in the n-drift region. The electrical equivalent circuit representing the even harmonics of the Fourier terms for the stored charge is illustrated in Fig. 2.

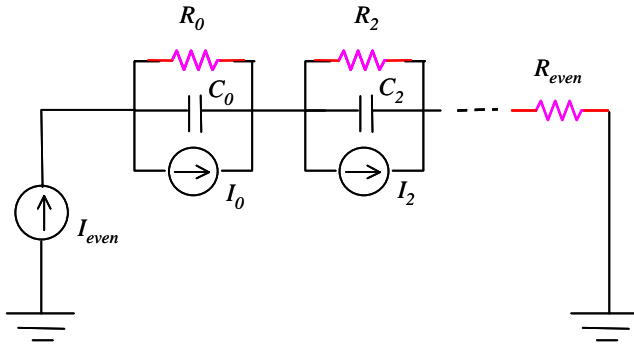


Fig. 2. Electrical equivalent circuit modeling the stored charge in the n-drift region (only even harmonics of the Fourier series solution of the ambipolar diffusion equation shown).

The terminating resistor,  $R_{even}$ , is the sum of the resistance of all the missing terms not included in the truncated series expansion. The shunt current sources are for moving boundaries of the drift region, and the driving current,  $I_{even} = D[g(t) - f(t)]$  is the current entering the diode unit-cell.

The current sources define the boundary conditions. The diode then appears as a controlled voltage source to the load in the circuit simulator. This controlled voltage source is made up of the junction drop across the p-emitter to n-drift,  $V_{J1}$ , drop across the stored charge region,  $V_b$ , the drop across

the depletion region around the p-emitter/n-base junction (the depletion region out from  $x_1$  at a depletion width  $W_{d1}$  away from  $x_1$ )  $V_{d1}$ , and the voltage across the depletion region out from  $x_2$  (depletion width  $W_{d2}$  away from  $x_2$ )  $V_{d2}$ . These simulate the total voltage drop along the main current path through the diode.

The forward drop,  $V_{AK}$ , is given by

$$V_{AK} = V_{J1} + V_b + V_{d1} + V_{d2} \quad (5)$$

where

$$V_{J1} = \frac{kT}{q} \ln \left( \frac{p_{x_1} p_{x_2}}{n_i^2} \right) \quad (6)$$

$$V_b = \frac{I_C}{\mu A q} \int_{x_1}^{x_2} p(x,t) dx \quad (7)$$

$$V_{d1} = \frac{q}{2\epsilon_{Si}} \left( N_B + \frac{I_C}{qA v_{sat}} \right) W_{d1}^2 \quad (8)$$

$$V_{d2} = \frac{q}{2\epsilon_{Si}} \left( N_B + \frac{I_C}{qA v_{sat}} \right) W_{d2}^2 \quad (9)$$

In (7)  $A$  refers to the Si area,  $\mu$  is the effective mobility given as the sum of the hole and electron mobilities, while in (8)  $N_B$  is the n-base doping concentration,  $v_{sat}$  is the saturation drift velocity, and  $I_C$  is the total anode current through the diode.

### C. PSpice implementation

The *pin* diode model described above can be implemented in circuit simulators such as the VTB or PSpice.

In the model, the Fourier series coefficients of the carrier density are calculated at every time step. From these coefficient calculations, substituted into (2), the carrier profile can also be calculated at every time step. The drift region voltage drop  $V_b$ , given by equation (7), is actually calculated from the discretized carrier profile shown in Fig.3. The carrier profile is assumed to be linear between two adjacent points. Considering the trade-off between simulation speed and accuracy, seven sampling points are typically used.

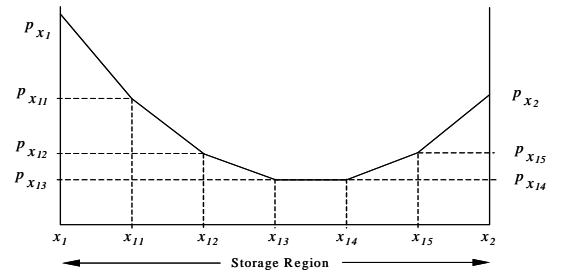


Fig. 3. Discretized carrier profile for simulation of  $V_b$ .

With this model, the dynamic switching behavior and static characteristics of *pin* diodes have been successfully

simulated. A typical simulation result for inductive switching is shown in Fig. 4, in which the direction of the voltage and current is defined along the diode positive direction. From the picture, it can be seen that the model captures both the reverse recovery current at diode turn-off, and the forward voltage overshoot during diode turn-on. The accuracy of the transient behavior will be shown later.

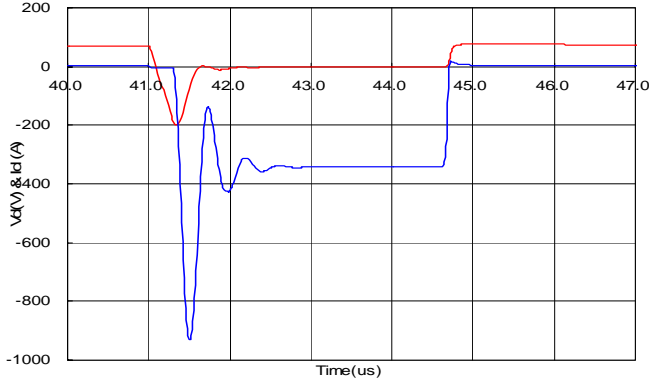


Fig. 4. Diode voltage (blue) and current (red) simulation waveforms.

In the model, the voltage drop  $V_0$  across the  $R_0C_0$  network in Fig. 2 represents the average carrier concentration  $p_0$  in (2), so it is easy to estimate the diode drift region charge with (10) during the simulation.

$$Q = q p_0 A W_b \quad (10)$$

where the  $A$  is the active die area,  $W_b$  is the width of the drift region, and  $q$  is the electron charge.

#### D. Electro-thermal model

Several dominant physical parameters associated with semiconductor devices are sensitive to temperature variations; causing their dependent device characteristics to change dramatically. The most important of these parameters are: *i*) the minority carrier lifetimes (which control the high-level injection lifetimes), *ii*) the hole and electron mobilities, *iii*) the free-carrier concentrations (primarily the ionized impurity-atom concentration), and *iv*) the intrinsic carrier concentration value,  $n_i$ . Almost all of the impurity atoms are assumed to be ionized at temperatures above 120 K (-150 °C) and are considered to be the impurity doping concentration values in the analysis.

Many empirical temperature dependencies of the carrier mobilities and recombination lifetimes are described in the literature [3-10]. The temperature dependencies used in this model are discussed in detail in [11], and the temperature dependent equations are given in Table 1. The high-level lifetime in (11) is given in seconds and the temperature in Kelvin.

The empirical relations used in the simulations, for electron and hole mobility as a function of temperature, are given by (12) and (13), respectively ( $T$  in Kelvin and  $\mu$  in

$\text{cm}^2/\text{V}\cdot\text{s}$ ). Auger recombination and carrier-carrier scattering effects are not included in the equations, but will be in the future. Based on the Einstein relation, the temperature dependence of the diffusion coefficients is related with that of mobilities.

The intrinsic carrier concentration,  $n_i$ , appears as a parameter in the simulation equations as well, and its temperature dependence is given by [21] in (14). It is a fair approximation for doping concentrations less than  $10^{17} \text{ cm}^{-3}$ . A more accurate expression for  $n_i$  that includes the temperature effects on the hole and electron density-of-states effective masses, bandgap narrowing, and a more exact solution to the Fermi integral, will all be included in future simulation results.

TABLE I  
TEMPERATURE DEPENDENCE OF MODEL PARAMETERS

Parameter	Temperature Dependence Equation
Carrier lifetime	$\tau_{HL} = 5 \times 10^{-7} \left( \frac{T}{300} \right)^{1.5}$ (11)
Electron mobility	$\mu_n = 1400 \left( \frac{300}{T} \right)^{2.5}$ (12)
Hole mobility	$\mu_p = 450 \left( \frac{300}{T} \right)^{2.5}$ (13)
Intrinsic concentration	$n_i = \frac{3.88 \times 10^{16} (T)^{1.5}}{\exp\left(\frac{7000}{T}\right)}$ (14)

The junction temperature during operation is determined using an equivalent electrical circuit as discussed by [12] and as shown in Fig. 5, in which four RC stages represent the thermal equivalent circuit models of the 4 major layers of the diode module: silicon die, ceramic and copper substrate, and aluminum heatsink.

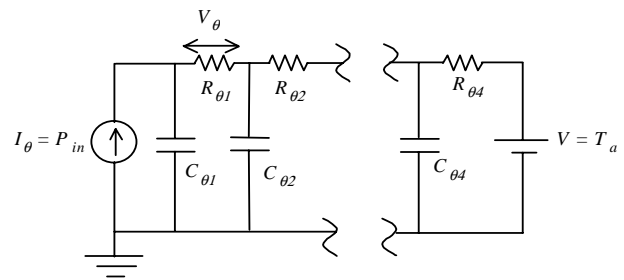


Fig. 5. Equivalent electrical circuit used for thermal modeling.

The temperature calculated from the thermal equivalent circuit is used to update the device temperature-dependant parameters, which are used in turn to calculate the new value of carrier concentration and voltage drops across the diode. The updated voltage drops are used to re-calculate the terminal voltages and currents through the diode.

### III. PARAMETER EXTRACTION

One of the major advantages of the model is that only four parameters from manufacturers are needed and can be easily estimated from the datasheets or from a single diode turn-off measurement. The four parameters of the electro-thermal physics-based model are:

- 1) Effective high level lifetime,  $\tau$
- 2) Active die area,  $A$
- 3) Drift region width,  $W$
- 4) Impurity doping density in the drift region,  $N_B$ .

Five important parameters given in the diode manufacturer datasheets are: *i*) repetitive maximum voltage,  $V_{RRM}$ , *ii*) dc forward current,  $I_F$ , *iii*) reverse recovery charge,  $Q_{RR}$ , *iv*) reverse recovery peak current,  $I_{RR}$ , and *v*) reverse recovery time,  $t_{RR}$ . The meaning of some of these parameters is illustrated in Fig. 6. The reverse recovery time is the sum of  $t_A$  and  $t_B$ .

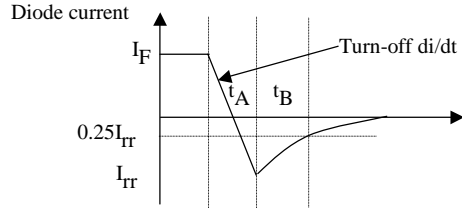


Fig. 6. Diode reverse recovery current.

The whole parameter extraction procedure in this work is divided into two stages: *i*) a rough estimation from the datasheet and *ii*) a refinement with a simple turn-off test. The steps are described below.

#### Stage i) – Initial Extraction of Parameter Values:

*a*) Since the maximum current density  $J$  is for most power diodes from  $100 \text{ A/cm}^2$  to  $150 \text{ A/cm}^2$ , the active die area  $A$  can be roughly estimated from the average forward DC current in the datasheet using (15).

$$A = I_F / J \quad (15)$$

*b*) Without the consideration of the recombination effect in the reverse charge, equation (16) is used to make a low estimation for the initial recovery time,  $\tau_0$ , which is the starting value for determining the effective high-level lifetime,  $\tau$ , to be used in the model.

$$\tau_0 = Q_{RR} / I_F \quad (16)$$

*c*) In the case that the reverse recovery charge  $Q_{RR}$  in the datasheet is given for a temperature other than room temperature, the parameter  $\tau_0$  can be scaled according to (11).

*d*) The electric field ( $E$ ) dependence of the ionization coefficients for electrons and holes in Si,  $\alpha$ , has been shown

to fit experimental data fairly well in the form as given in (17), [13-15],

$$\alpha_{n,p} = \alpha \exp(-b / E) \quad (17)$$

where  $a$  varies between  $7 \times 10^5$  and  $3.8 \times 10^6 \text{ cm}^{-1}$  with a corresponding variation in  $b$  from  $1.47 \times 10^6$  to  $1.75 \times 10^6 \text{ V/cm}$ . Assuming breakdown in the bulk, an abrupt junction, equal ionization coefficients for holes and electrons, and a  $p^+-n^-n^+$  structure, an expression for the breakdown voltage in terms of the parameters  $a$ ,  $b$ , and the n-base width,  $W$ , can be obtained (18).

$$V_{BD} = \frac{bW}{\ln(aW)} \quad (18)$$

The n-base width,  $W$ , used in the model is derived based on (18) using  $a = 1.07 \times 10^6 \text{ cm}^{-1}$ ,  $b = 1.65 \times 10^6 \text{ V/cm}$ , and the value of the breakdown voltage from the manufacturer's data sheet plus some margin.

*e*) For purposes of the modeling and based on the empirical effective impurity doping concentration range ( $6 \times 10^{13} - 2 \times 10^{14} \text{ cm}^{-3}$ ) in n-drift region, the doping concentration is assumed to be  $10^{14} \text{ cm}^{-3}$ .

So far, all the parameters needed for the model have been estimated. In order to increase the accuracy of parameter extraction, a refinement based on an inductive diode turn-off measurement at room temperature is necessary.

#### Stage ii) – Refinement of Parameter Values:

*f*) Using (19) and the  $di/dt$  measurement value, the parasitic inductance in the switching loop of the circuit is calculated.

$$L_e = V_{ss} / di / dt \quad (19)$$

*g*) With the values of  $Q_{RR}$  and  $I_F$  obtained from the measurements, repeat step *b*) to improve the estimate of the initial recovery time  $\tau_0$ .

*h*) Improvement of the parameter estimates by running simulations using the model can be made by trying to match the experimental results. The following observations give some guidelines on how to proceed. In the model, the effective lifetime is the dominant parameter affecting the reverse recovery current and voltage waveforms. With the correct high-level lifetime  $\tau$ , not only good matching of the reverse current can be obtained, but also a good match of the diode voltage waveform during turn-off, including overshoot and ringing, can be made. The first estimate of high-level lifetime,  $\tau$ , is given by the initial recovery time  $\tau_0$ . A better estimate can be obtained by trying to match the reverse recovery current. After this, the n-base width estimate can be improved by trying to improve the matching of the diode voltage waveform. It has been found empirically that, compared with lifetime  $\tau$ , the width and doping of the n-drift region do not have significant effects on the reverse recovery current, but have an obvious effect on the diode voltage waveform in the simulation.

## IV. EXPERIMENT AND SIMULATION

### A. Diode testing experiment

In order to validate the proposed approach, two fast-recovery power diodes from different manufacturers were tested. Parameters  $I_{FM}$  and  $V_{RRM}$  from the datasheets and parameters  $R_{on}$  and  $V_{BR}$  obtained from static testing are given in Table II.

The static characteristic (on-state voltage drop  $V_{on}$  and breakdown voltage  $V_{BR}$ ) testing was performed with a standard curve tracer. The testing results showed that the on-state resistances of both diodes was around 20 m $\Omega$ , and the non-repetitive breakdown voltages  $V_{BR}$  of both diodes are almost one-third bigger than the datasheet values of  $V_{RRM}$ . Therefore, the actual value of  $V_{BR}$  (margin) needs to be considered for more accurate parameter extraction.

TABLE II  
MAXIMUM RATINGS AND STATIC TESTING RESULTS

Diode	$I_{FM}$ (A)	$V_{RRM}$ (V)	$R_{on}$ (m $\Omega$ )	$V_{BR}$ (V)
A	100	600	17	900
B	81	1000	19	1500

The diode turn-off experiments were performed with a typical chopper circuit, shown in Fig. 7. In the circuit, the switch is implemented with a 1200V/600A IGBT, and in order to avoid damage to the devices due to the voltage overshoot, a 3.4  $\Omega$ , 9.4 nF RC-snubber was placed in parallel with the diode. Because of the small values of the snubber resistance and capacitance, the variation in component values with respect to temperature change could be neglected in so far as these variations might alter the diode switching waveforms. The diode was placed in an environmental chamber so that the operating temperature could be varied.

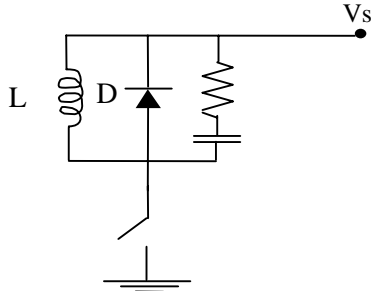


Fig. 7. Diode switching test circuit.

The diode turn-off waveforms were recorded at several temperatures from  $-150$  to  $200$   $^{\circ}\text{C}$  in increments of  $50$   $^{\circ}\text{C}$ . The forward diode current was 70 A and the supply voltage was 350 V for all measurements. This testing was performed three times to validate the repeatability of the switching waveforms obtained. Since it was not possible to place the current probe in the environmental chamber, and yet it was desirable to place the RC snubber circuit as close to the diode as possible, only the total current of the diode together with the snubber branch could be directly measured in the experiment. The final diode current was obtained by subtracting the calculated snubber current. This post-

processing of the diode current waveform was responsible for some of the high-frequency noise in the diode current waveform.

Based on (19), the stray inductance in the test circuit was calculated to be 330 nH. The main parameters describing the reverse recovery current waveform were defined in Fig.6. Measured values obtained from the experimental waveforms at various temperatures are summarized in Table III.  $I_{rr}$ ,  $t_a$ ,  $t_b$  and  $t_{rr}$  in Table III correspond to the symbol definitions illustrated in Fig. 6.

TABLE III  
MEASUREMENT RESULTS OF THE REVERSE RECOVERY CURRENTS AT DIFFERENT TEMPERATURES

Diode	Temp	$I_{rr}$ (A)	$t_a$ ( $\mu\text{s}$ )	$t_b$ ( $\mu\text{s}$ )	$t_{rr}$ ( $\mu\text{s}$ )
A	$-150$ $^{\circ}\text{C}$	53	0.055	0.09	0.145
	$27$ $^{\circ}\text{C}$	118	0.12	0.12	0.24
	$150$ $^{\circ}\text{C}$	144	0.15	0.18	0.33
B	$-150$ $^{\circ}\text{C}$	79	0.08	0.07	0.15
	$27$ $^{\circ}\text{C}$	229	0.23	0.14	0.37
	$150$ $^{\circ}\text{C}$	284	0.3	0.19	0.49

### B. Comparison of the experimental and simulation results

The model parameters for the two diodes are estimated using the parameter extraction procedure described above. Since the diode turn-off behavior is of more concern to engineers than the turn-on, only the simulation results for diode turn-off are shown. The turn-off waveform comparisons of diode A at room temperature,  $-150$   $^{\circ}\text{C}$ , and  $150$   $^{\circ}\text{C}$  are shown in Figs. 8, 9 and 10, respectively. The horizontal scale is 500 ns/div in all the figures shown below. The current scales are in Amperes and the voltage scales are in Volts.

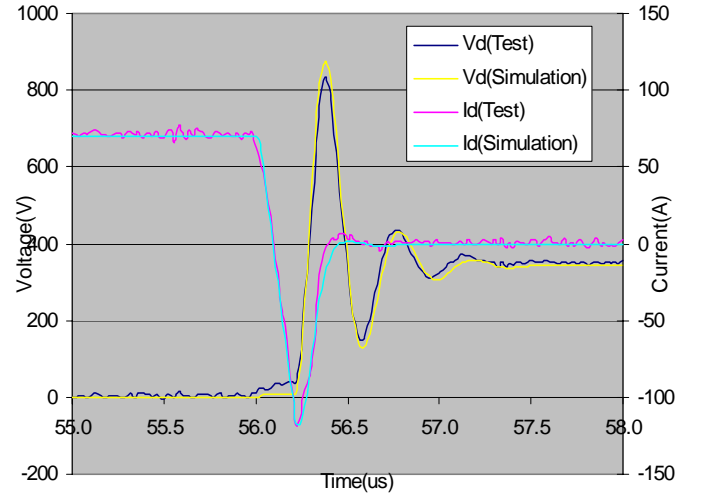


Fig. 8. Diode A at room temperature. Comparison between the experimental result (dark blue-voltage & pink-current) and simulation (yellow-voltage & light blue-current) during turn-off.

The very close match between the simulation and the experimental results shown in the Fig. 8 proves the

robustness of the parameter extraction procedure and accuracy of the model.

In the experimental voltage waveform (dark blue), it can be seen that the diode voltage starts increasing and reaches a small value (about 30 V) before the reverse current reaches its maximum  $I_{rr}$ . This voltage drop is caused by the parasitic inductance in the diode package. The small inductive voltage drop in the simulated voltage waveforms is due to an embedded 7 nH inductance in the model (representing the stray package inductance). The instant in time the anode current reaches  $I_{rr}$ , the depletion region in the n-base first appears and the diode begins to support the applied reverse voltage.

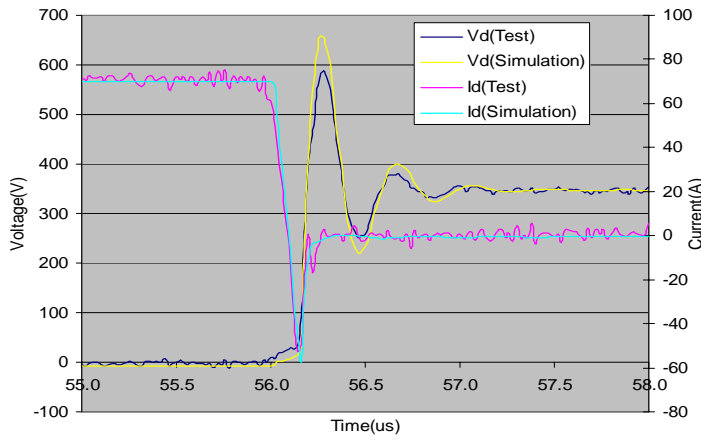


Fig. 9. Diode **A** at  $-150\text{ }^{\circ}\text{C}$ . Comparison between the experimental result (dark blue-voltage & pink-current) and simulation (yellow-voltage & light blue-current) during turn-off.

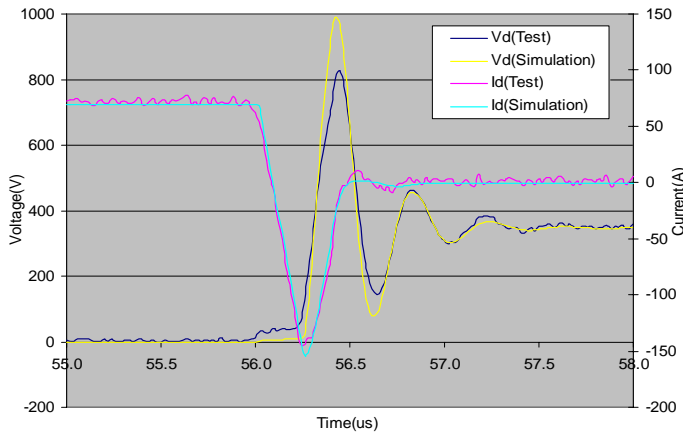


Fig. 10. Diode **A** at  $150\text{ }^{\circ}\text{C}$ . Comparison between the experimental result (dark blue-voltage & pink-current) and simulation (yellow-voltage & light blue-current) during turn-off.

At the temperatures  $-150\text{ }^{\circ}\text{C}$  and  $150\text{ }^{\circ}\text{C}$ , the simulation still shows excellent matching with the experimental results, especially for the reverse recovery current. The errors between the simulated and experimental voltage oscillations and rate of damping are most likely the result of some inaccuracies in the modeling of the diode capacitances.

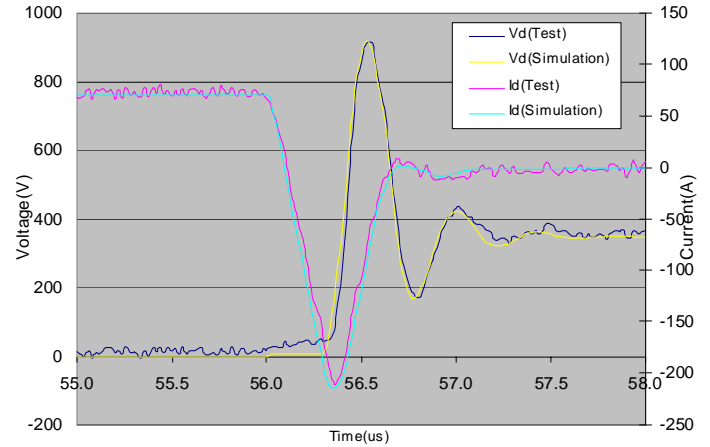


Fig. 11. . Diode **B** at room temperature. Comparison between the experimental result (dark blue-voltage & pink-current) and simulation (yellow-voltage & light blue-current) during turn-off.

The turn-off waveform comparisons of diode **B** between the experimental and simulation results at room temperature,  $-150\text{ }^{\circ}\text{C}$  and  $150\text{ }^{\circ}\text{C}$  are shown in Figs. 11, 12 and 13, respectively. The similarity between the actual and simulated waveforms again shows the model accuracy and robustness over a wide temperature range.

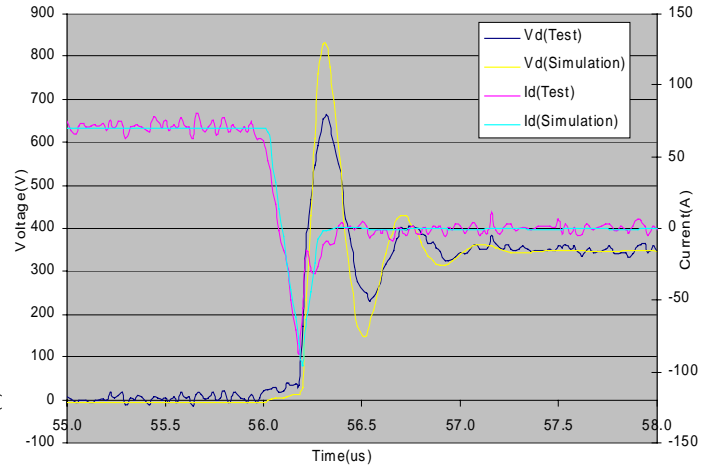


Fig. 12. Diode **B** at  $-150\text{ }^{\circ}\text{C}$ . Comparison between the experimental result (dark blue-voltage & pink-current) and simulation (yellow-voltage & light blue-current) during turn-off.

## V. CONCLUSIONS

The satisfactory simulation results strongly prove the accuracy of the electro-thermo, physics-based diode model, and the possibility of a simple parameter extraction methodology using the manufacturer's datasheets as well as the refinement possible with one simple measurement. The simplicity of the parameter extraction method presented here further increases the practicality of the model for the circuit designer.

The work also demonstrates the most important manufacturer's parameters used in the model. These are primarily concerned with the diode reverse recovery period. The effective lifetime is the most important model parameter

and it determines the reverse recovery current waveform. The n-base width and impurity doping concentration of the n-base (drift) region primarily affect the voltage overshoot during turn-on and turn-off. The model parameter refinement, from the measured reverse recovery voltage waveform in the simulation at room temperature, indicates the need to improve the model with respect to diode capacitance effects. Finally, the fast computer run times are consistent with the desire to use such a detailed model in circuit simulations.

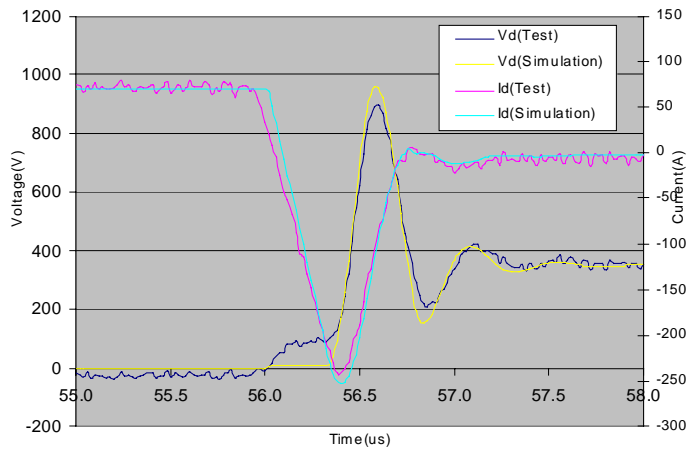


Fig. 13. Diode **B** at 150 °C. Comparison between the experimental result (dark blue-voltage & pink-current) and simulation (yellow-voltage & light blue-current) during turn-off.

## REFERENCES

- [1] Leturcq, Berraies, Debrie, Gillet, Kallala and Massol, "Bipolar semiconductor device models for computer-aided design in power electronics," *6th European Conference on Power Electronics*, vol. 2, p. 84, Sept. 1995.
- [2] P.R. Palmer, J.C. Joyce, P.Y. Eng, J.L. Hudgins, E. Santi, and R. Dougal, "Circuit simulator models for the diode and IGBT with full temperature dependent features," *IEEE PESC Rec.*, pp. , June 2001.
- [3] B.J. Baliga and S. Krishna, "Optimization of recombination levels and their capture cross-section in power rectifiers and thyristors," *Solid-State Electronics*, vol. 20, pp. 225-232, 1977.
- [4] C. Canali, G. Majni, R. Minder, and G. Ottaviani, "Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature," *IEEE Trans. ED*, pp. 1045-1047, November 1975.
- [5] C. Jacoboni, C. Canali, G. Ottaviani, and A. Alberigi-Quaranta, "A review of some charge transport properties of silicon," *Solid-State Electronics*, vol. 20, pp. 77-89, 1977.
- [6] N.D. Arora, J.R. Hauser, and D.J. Roulston, "Electron and hole mobilities in silicon as a function of concentration and temperature," *IEEE Tran. ED*, vol. 29, pp. 292-295, February 1982.
- [7] C. Canali, C. Jacoboni, F. Nava, G. Ottaviani, and A. Alberigi-Quaranta, "Electron drift velocity in silicon," *Physical Rev. B*, vol. 12, no. 4, pp. 2265-2284, August 1975.
- [8] G. Ottaviani, L. Reggiani, C. Canali, F. Nava, , and A. Alberigi-Quaranta, "Hole drift velocity in silicon," *Physical Rev. B*, vol. 12, no. 8, pp. 3318-3329, October 1975.
- [9] H. Schlangenotto and W. Gerlach, "On the effective carrier lifetime in *p-s-n* rectifiers at high injection levels," *Solid-State Electronics*, vol. 12, pp. 267-275, 1969.
- [10] A.R. Hefner Jr., "A dynamic electro-thermal model for the IGBT", *IEEE Trans. IA*, vol. 30, no. 2, pp. 394-405, 1994.
- [11] E. Santi, A. Caiafa, X. Kang, J.L. Hudgins, P.R. Palmer, D. Goodwine, and A. Monti "Temperature effects on trench-gate IGBTs," *IEEE IAS Annual Mtg. Rec.*, in press, Oct. 2001.
- [12] Ammous, Ghedira, Allard, Morel and Renault, "Choosing a thermal model for electrothermal simulation of power semiconductor devices," *IEEE Trans. PEL*, vol. 14, no. 2, pp. 300-307, 1999.
- [13] R. Van Overstraeten and H. DeMan, "Measurements of the ionization rates in diffused silicon p-n junctions," *Solid State Electronics*, vol. 13, no. 5, pp. 583-608, 1970.
- [14] R.A. Kokosa and R.L. Davies, "Avalanche breakdown of diffused silicon p-n junctions," *IEEE Trans. ED*, vol. 13, no. 12, pp. 874-881, 1966.
- [15] S.M. Sze and G. Gibbons, "Avalanche breakdown voltages of abrupt and linearly graded p-n junctions in Ge, Si, GaAs, and GaP," *Appl. Phys. Lett.*, vol. 8, p.111, 1966.