Parameter Extraction Procedure for Vertical SiC Power JFET

Abstract—A practical parameter extraction procedure for a power silicon carbide (SiC) junction field-effect transistor (JFET) is presented. The carrier mobility and carrier concentration are very important parameters, strongly affecting the device current capability and dynamic characteristics for a given design. When modeling JFETs, the values of these parameters are usually based on assumptions and given by a vendor in a range. As a result, model accuracy is compromised. In this paper, a step-by-step parameter extraction procedure is described that includes the extraction of mobility and carrier concentration in the channel and drift regions based on knowledge of device geometrical parameters. For the first time, carrier mobilities in the channel and drift regions of a power JFET are extracted individually. It is found that channel and drift region mobilities can be very different for a given device since they are strongly dependent on the fabrication process. The separate extraction of these two mobilities can also improve model accuracy in the case of imperfect knowledge of the device geometry. The developed procedure includes the extraction of empirical parameters describing the temperature dependence of mobilities in the channel and drift regions. A simple static I–V characterization and C–V measurements are the only measurements required for the parameter extraction. In this paper, the procedure is experimentally validated for both normally off (enhancement mode) and normally on (depletion mode) JFETs.

Index Terms—junction field-effect transistor (JFET) switches, parameter extraction, power semiconductor devices, silicon carbide JFETs.

I. INTRODUCTION

Silicon carbide (SiC) is one of the most promising semiconductor materials for next-generation power semiconductor devices. Currently, significant improvements in SiC material and device fabrication have been made so that high-power SiC devices such as MOSFETs and junction field-effect transistors (JFETs) are expected to appear in the market in the near future [1]. Since SiC high-power devices are still under development, there is a need to create accurate and validated models for SiC prototype devices to allow power converters to predict the impact of the new devices on system performance and facilitate device commercialization. To make a model practical, it is very important to provide the extraction procedure for the parameters employed in the model description. While comprehensive techniques for MOSFET parameter extraction have been developed, very limited work has been done for the high-power JFET. This can be explained by the fact that silicon (Si) JFETs are used for very low power applications and the power Si JFET appeared on the market for only a short time before being replaced by the more advanced power MOSFET model.

Generally, SiC device electrical models use an empirical expression for carrier mobility such as (1) [2], [3], despite the fact that it is well known that this parameter may vary over quite a wide range, depending on processing parameters such as temperature, annealing conditions, defect density, stoichiometry, and so on [4]–[6].

\[
\mu(T) = \frac{947 \cdot (N_0 \cdot T_{300})^{0.61} \cdot (T)}{1 + (N_0 \cdot T_{300})^{0.61} \cdot (T)}^{2.15}.
\]

In a power JFET, both the channel and the drift region 62 give significant contribution to the device on-resistance and, consequently, to the forward voltage drop during forward operation. Therefore, it is important to consider these regions as two individual regions with different electrical properties. First, the carrier concentration in the drift region is typically an order of magnitude lower than that in the channel region, which consequently results in higher carrier mobility in the drift region. Second, carrier mobility in the drift region can vary in quite a wide range, depending on the growth method [4] [sublimation or chemical vapor deposition (CVD)] and 72 doping process used to achieve the semi-insulating property 73 of the blocking layer. There are basically two techniques to 74 fabricate semi-insulating SiC material: the high-purity semi-insulating (HPSI) process, where low unintentional doping is 76 obtained by means of purification of gasses, growth chamber, 77 etc., and the vanadium-doped semi-insulating (VDSI) process, 78 where unwanted donor doping is compensated by the introduc- 79 tion of vanadium atoms. It was demonstrated that the carrier 80...
AQ1

81 mobility of the HPSI material can be twice as high as that
82 of the VDSI material, 113 cm²/V·s versus 66.9 cm²/V·s,
83 respectively [5]. It was shown in [6] that the C/Si ratio during
84 CVD growth of semi-insulating SiC significantly affects the
85 trap density and controlling this parameter makes it possible to
86 grow an ultrahigh purity SiC material with a carrier mobility of
87 981 cm²/V·s.

From a device modeling standpoint, carrier mobility is an
89 important parameter determining the current capability of the
90 device for a given design. Small changes in mobility signif-
91 icantly affect device characteristics, and for the accurate predic-
92 tion of the electrical behavior, this parameter has to be known
93 precisely. In this paper, for the first time, carrier mobilities in the
94 channel and the drift region of a power JFET are extracted in-
95 dividually. This is important because the two mobilities can be
96 significantly different, depending on fabrication, as explained
97 earlier. Another advantage of the proposed procedure is that
98 the carrier concentrations in the channel and in the drift region
99 are also considered as technological parameters and are explic-
100 itly extracted. These carrier concentrations, as the mobilities
101 discussed earlier, have a significant effect on device behavior
102 and are not precisely known. The uncertainty comes again
103 from fabrication and also from incomplete dopant ionization at
104 ambient temperature—the so-called carrier freezing in SiC.

The JFET operation is briefly reviewed in Section II, and
106 the proposed parameter extraction procedure is described in
107 Section III and experimentally validated in Section IV for both
108 normally off and normally on JFETs.

II. BRIEF REVIEW OF JFET OPERATION

A compact physics-based model for a vertical power SiC
111 JFET with the structure shown in Fig. 1 was recently developed
and validated [7]. In this section, device operation is described
112 with reference to this model in order to identify the required
113 physics-based parameters to be extracted. However, the device
114 parameters obtained from this extraction procedure could be
115 used with a different physics-based JFET model. Please note
116 that the procedure as described applies to the vertical JFET
117 structure of Fig. 1. Modifications of this extraction procedure to
118 apply it to lateral-channel JFETs [8] are possible but are outside
119 the scope of this paper.

The modeling is applied to an equivalent single-cell structure
120 as shown in Fig. 1. An actual power JFET is a large area
121 device, and it is usually realized as a grid of individual cells
122 connected in parallel by top metallization. For simplicity of
123 model description, the real structure is replaced by a single
124 cell with a length Z (perpendicular to the page) equal to the
125 sum of the lengths of all individual grid cells. The basic device
126 dimensions are the channel length \( L \), the channel width \( 2a \),
127 the drift region length \( W_{\text{Drift}} \), and the drift region length \( 129
\)

\( L_{\text{Drift}} \). There is no structural difference between a normally
130 on and a normally off JFET. This property of the JFET is
131 determined by the width of the channel region and its doping
132 concentration only. Depending on the application goal, these
133 two parameters can be designed in such a way that the channel
134 is fully depleted (normally off) or partially depleted (normally
135 on) under zero gate bias condition.

Output characteristics of the JFET exhibit two distinct oper-
137 ating regions: the linear region in which the channel current is
138 approximately proportional to the channel voltage and the satu-
139 ration region in which the channel current is approximately con-
stant. In the linear region, corresponding to small drain–source
140 voltage, the depleted region of the channel is determined by the
141 gate–source voltage, and it has an approximately uniform width
142 along the channel. The following equation describes the JFET
144 electrical behavior in the linear region:

\[
I_{\text{CH}} = I_P \left\{ \frac{3V_{\text{CH}}}{V_P} - \frac{2}{V_P} \left( V_{\text{CH}} - V_{\text{GS}} + V_{\text{bi}} \right)^2 \right\} \left( \frac{1}{1+\lambda(V_{\text{CH}} - V_{\text{CHSAT}})} \right).
\]

\]

In this equation, \( I_{\text{CH}} \) is the channel current, which is equal to
146 the JFET drain current, \( V_{\text{CH}} \) is the channel voltage, \( V_{\text{GS}} \) is the
147 gate–source voltage, \( V_{\text{bi}} \) is the built-in voltage, \( I_P \) is the discharge
148 pinchoff current, and \( V_P \) is the pinchoff voltage.

With further increase of channel voltage, the depletion region
150 becomes progressively wider toward the drain side (see Fig. 1)
151 causing a reduction of channel width and an increase of channel
152 resistance. As a result, JFET current saturates. Another possi-
153 ble reason for current saturation is carrier velocity saturation
154 due to the presence of high electric field in the channel. In 155
the saturation region, the electrical behavior of the device is 156
described by

\[
I_{\text{CHSATE}} = I_P \left\{ 1 - \frac{3V_{\text{bi}} - V_{\text{GS}}}{V_P} + 2 \left( \frac{V_{\text{bi}} - V_{\text{GS}}}{V_P} \right)^2 \right\} \times [1 + \lambda(V_{\text{CH}} - V_{\text{CHSATE}})].
\]

\]
Pinchoff current \( I_p \) and pinchoff voltage \( V_p \) are defined as

\[
I_p = \frac{Z \cdot \mu_p \cdot q^2 \cdot N_{CH}^2 \cdot a^3}{3 \varepsilon_{SiC} \cdot L_{eff}} \tag{4}
\]

\[
V_p = \frac{q \cdot N_{CH} \cdot a^2}{2 \cdot \varepsilon_{SiC}} \tag{5}
\]

where \( \varepsilon_{SiC} \) is the dielectric constant of SiC.

An empirical constant parameter \( \lambda \), called the channel-length modulation coefficient, determines the increase of current in the saturation region in (3) and can be extracted from the slope of \( I-V \) characteristics in the saturation region [9]. The boundary between the linear and the saturation region is given by the saturation voltage \( V_{CHSAT} \), which is the channel voltage at which the JFET enters the saturation region. This voltage is a linear function of the applied gate voltage and is given by

\[
V_{CHSAT} = V_p + V_{GS} - V_{bi}. \tag{6}
\]

The voltage \( V_{CH} \) is the effective voltage applied to the channel, and it is equal to the drain–source voltage reduced by the drift region voltage drop

\[
V_{CH} = V_{DS} - I_{CH} R_{DRIFT} \tag{7}
\]

where drift region resistance is given by

\[
R_{DRIFT} = \frac{L_{DRIFT}}{q \cdot \mu_{DRIFT} \cdot N_{DRIFT} \cdot Z \cdot W_{DRIFT}}. \tag{8}
\]

From (3)–(5), it can be concluded that one of the most important parameters which establishes the current level in the saturation regime is the channel half width \( a \), which appears cubed in (4) and squared in (5). The on-resistance of the JFET in the linear region is determined mostly by carrier mobilities in the channel and drift regions. In order to predict the device behavior in the full range of the operational conditions, it is necessary to establish temperature dependences of mobility in the channel and drift regions. These mobilities can be described by empirical equations similar to (1). As part of the proposed parameter extraction procedure, the extraction of parameters describing the temperature dependence of mobilities will be discussed.

Table I shows the complete list of JFET parameters and the technique used for extraction. The first four geometrical parameters are assumed to be known for the proposed parameter extraction procedure. A fifth geometrical parameter, the drift region length \( L_{DRIFT} \), may be assumed to be known or can be extracted from breakdown voltage measurements.

### III. Parameter Extraction Procedure

The parameter extraction approach discussed in this paper is based on the assumption that device geometrical parameters \( a, L, Z, \) and \( W_{DRIFT} \) are known. Channel-length modulation coefficient \( \lambda \) is extracted from the slope of \( I-V \) characteristics in the saturation region [9]. The experimental measurements shown in this section have been made on a normally off JFET sample provided by SemiSouth.

### A. Drift Region Parameters \( N_{DRIFT}, L_{DRIFT} \)

\( C-V \) measurements can be performed to extract drift region carrier concentration \( N_{DRIFT} \). The measurement setup is shown in Fig. 2(a).

A negative gate bias is needed for a normally on device to provide complete depletion of the channel. For a normally off device, this condition is already satisfied with zero gate bias by internal device design. When the channel is fully off, the depletion region is located entirely inside the drift region, and the depletion boundary cross section, which represents the area of the equivalent capacitor, corresponds to the known effective area of the device. Referring to Fig. 1, the depletion layer edge is a horizontal line located within the drift region. Given the trench gate structure of the device of Fig. 1 with the gate terminal extending toward the drain and “shielding” the source terminal, it is expected that the gate–drain capacitance will turn out to be much larger than the drain–source capacitance. This is confirmed by \( C-V \) measurements that show a drain–source capacitance of 2–3 pF. Therefore, the capacitance between the gate and the drain can be represented by a capacitor having plates with an area \( A = Z \cdot W_{DRIFT} \) (see Fig. 1) and 219 spacing between them equal to the depleted width of the drift region \( W_D \)

\[
C_{GD} = \frac{\varepsilon_{SiC} Z \cdot W_{DRIFT}}{W_D}. \tag{9}
\]

On the other hand, to deplete a thickness \( W_D \) of semiconductor material having carrier concentration \( N_{DRIFT} \), the required
Substituting (10) into (9), an expression for carrier concentration as a function of applied voltage and corresponding capacitance can be obtained

\[
N_{\text{DRIFT}} = \frac{2(V_{DS} + V_{bh})C_{GD}^2}{q\varepsilon_{SiC}Z^2W_{\text{DRIFT}}^2}.
\] (11)

Note that (11) is valid only under the assumption that the drift region is uniformly doped. In the case of nonuniform dopant distribution in the drift region, its profile along the drift region can be estimated by [10]

\[
N_{\text{DRIFT}}(W_D) = \frac{2}{q\varepsilon_{SiC}Z^2W_{\text{DRIFT}}^2} \frac{d(1/C_{GD}^2)}{dV_{DS}}.
\] (12)

Keithley CV analyzer 590 was used to perform measurements in this paper. The output voltage of the analyzer was applied to the drain of the tested JFET, and the input of the analyzer was connected to the gate of the device to measure the displacement current of the gate–drain capacitance as shown in Fig. 2(a). Progressively increasing the drain bias voltage during the measurement, the capacitance is measured by superimposing a small ac voltage component. From (11), one can see that, if the drift region carrier concentration is constant, the quantity \(1/C_{GD}^2\) varies linearly with drain–source voltage \(V_{DS}\). From the plot in the inset of Fig. 2(b), two distinct slopes can be identified. This indicates that, for the studied JFET, the drift region contains two distinctive regions with different doping concentrations. At a depth of approximately 1.4 \(\mu\)m from the channel edge, the carrier concentration in the drift region reaches its lowest value and remains constant. There are two possible reasons for nonuniform carrier distribution in the drift region. First, there may be a transition layer intentionally formed between the drift and channel regions to reduce stress introduced by materials with different concentrations of dopant. Second, the depletion edge surface may not be flat when it approaches the channel region, thus changing the effective area of the plates of capacitance \(C_{GD}\). Extracting drain region carrier concentration at higher values of \(V_{DS}\) gives a more accurate result because the edge of the depletion region is absolutely flat while it starts to be deformed when approaching the channel region. Knowing the capacitance at a given drain–source voltage, the depletion width, introduced by this voltage, is calculated using (10), and then, the carrier distribution along the drift region is calculated using (12). The result is shown in Fig. 2(c) for the region corresponding to drain–source voltages between 20 and 40 V, which correspond to a region far into the drift region.

Nondestructive breakdown voltage measurements can be performed to evaluate drift region length \(L_{\text{DRIFT}}\). Slowly increasing the drain–source reverse bias and carefully monitoring the sudden increase in leakage current, the breakdown voltage for a given structure is estimated. To optimize the high-power device in both the forward and the reverse regime of operation, the drift region design is a tradeoff between high blocking capability and low on-resistance. The punched-through structure is commonly used to improve this tradeoff, because the desired...
Fig. 3. Transfer characteristic of normally off JFET.

Fig. 4. (a) Input capacitance measurement setup. (b) C–V measurements of input capacitances.

Fig. 5. Output characteristics of normally off SiC JFET.

Fig. 6. Extracted and simulated mobilities of JFET as a function of temperature. Ambient temperature is 300 K, and elevated temperature $T_1$ is 375 K.

$L_{DRIFT}$ can be obtained by solving the breakdown voltage equation [9]

$$V_{PT} = \frac{E_{crit}}{2} \left( 2L_{Drift} - \frac{L^2_{Drift}}{W_{dep}} \right)$$

(13)

where $W_{dep}$ is the depletion width for a non-punched-through design

$$W_{dep} = \frac{\varepsilon_{SiC}}{qN_{Drift}} E_{crit}.$$  

(14)

B. Channel Carrier Concentration $N_{CH}$

In order to extract the carrier concentration in the channel, one can proceed as follows: First, extract the threshold voltage $V_{TH}$ either from the device transfer characteristics or from a $C_{GS} - C_{GD}$ measurement, and then, use this value to calculate the pinchoff voltage $V_P$; finally, use (5) to calculate the channel carrier concentration from the calculated $V_P$. 

274 blocking voltage can be obtained with a smaller drift region thickness, with an associated smaller ON-state resistive drop. Assuming a punched-through design, the drift region thickness...
The threshold voltage $V_{TH}$ is extracted from the transfer characteristics of the device as shown in Fig. 3 (for details about threshold voltage extraction, see [11]). Alternatively, the threshold voltage can be extracted using a capacitance measurement technique, evaluating the change of $C_{GS}$ and $C_{GD}$ as a function of the applied gate–source voltage while keeping the drain and the source shorted (see Fig. 4(a) for setup details). When voltage increases, $C_{GD}$ gradually increases due to the reduction of the depleted portion of the drift region. At the moment when the gate voltage corresponds to the threshold value, the channel opens, and $C_{GD}$ abruptly drops down due to the reduction of the effective area of the plates of the $C_{GD}$ capacitance as shown in Fig. 4(b). At the same time, capacitance $C_{GS}$ abruptly increases due to channel opening. Note that, when the gate–source voltage is below the threshold value, $C_{GS}$ remains almost constant because of the fully depleted channel region.

Threshold voltage can be considered as the value of the gate–source voltage for which the saturation voltage is zero (the forward characteristic for $V_{GS} = V_{TH}$ has no linear region and 307 saturates at zero drain–source voltage). Therefore, substituting $V_{GS} = V_{TH}$ and $V_{CHSAT} = 0$ in (6), the pinchoff voltage is given by

$$V_p = V_{bi} - V_{TH}.$$  
\(15\)

Only two parameters, the width of the channel region and its doping concentration, determine the pinchoff voltage of a device. The pinchoff voltage for both normally on and normally off devices can be evaluated from (15), where $V_{TH}$ is the threshold voltage or external voltage applied to the gate in order to open the channel for conduction. The difference between the normally on and normally off devices is that, for a normally off JFET, built-in voltage $V_{bi}$ of the gate–source junction is sufficient to fully deplete the channel and the threshold voltage is positive while, for a normally on device, built-in voltage $V_{bi}$ only partially depletes the channel and the threshold voltage is negative because an additional reverse bias is needed to fully deplete the channel. The pinchoff voltage is positive for both structures. Using (5), the carrier concentration in the channel is calculated as

$$N_{CH} = \frac{2V_P\varepsilon_{SiC}}{qa^2}. \quad (16)$$

### C. Channel Mobility $\mu_{CH}$ and Drift Region Mobility $\mu_{DRIFT}$

The channel mobility can be extracted from the linear region of the output characteristics of the JFET, assuming that the channel and the drift layer can be represented as two rectangular-shaped regions of constant cross section. Neglecting contact resistance, the on-resistance of the JFET can be represented as the sum of the channel and drift region resistances

$$R_{ON} = R_{CH} + R_{DRIFT} = \frac{L}{2q\mu_{CH}N_{CH}Z(a - W_S)} + \frac{L_{DRIFT}}{q\mu_{DRIFT} Z \cdot W_{DRIFT}}. \quad (17)$$
where $W_S$ is the width of the depletion region between the source and the gate (see Fig. 1)

$$W_S = \sqrt{\frac{2\varepsilon_{SiC}(V_{bi} - V_{GS})}{qN_{CH}}}. \quad (18)$$

The lowest on-resistance occurs when the channel is completely open for current transport ($V_{GS} = 3\,V$ for the 4H-SiC normally off device), and the drain voltage is small ($V_{GS} \gg V_{DS}$), which ensures that the channel cross section is uniform along the entire channel length. The drift region of a power JFET is made relatively thick to support high blocking voltage, so that it can be assumed that the effective drift region cross section does not change significantly under low $V_{DS}$. In other words, current spreading effects where the channel meets the drift region can be neglected. Thus, the difference in initial ($V_{DS} \sim 0$) on-resistance of two curves in the family of static characteristics of the device is determined only by the change of channel resistance, while drift region resistance is a constant for any gate voltage. The carrier mobility in the channel can be extracted using two $I$–$V$ curves corresponding to different gate biases as shown in Fig. 5. The inverse of the slope around the origin of a forward characteristic gives the ON-state resistance for a given gate bias. Two such resistances $R_{ON1}$ and $R_{ON2}$ are shown in Fig. 5. Using (17) for the two resistances and subtracting the expressions so obtained, the drift resistance cancels out, and after rearranging, one obtains the desired expression for mobility

$$\mu_{CH} = \frac{L(W_{S1} - W_{S2})}{2qN_{CH}Z(R_{ON1} - R_{ON2})(a - W_{S1})(a - W_{S2})}. \quad (19)$$

Note that this derivation neglects the reduction of the drift region thickness and the extension of the channel into the drift region. Also, note that the measured drift region resistance includes the series substrate resistance. The substrate resistance of the studied normally off JFET is approximately 0.02 $\Omega$ while the on-resistance of the device is 0.2 $\Omega$. This means that the carrier mobility in the drift region is estimated with an error of 10%. Accurate carrier mobility in the drift region can be calculated, if needed, by correcting for the constant substrate resistance.

Carrier mobility in the drift region can then be calculated using the $I$–$V$ curve corresponding to fully open channel

$$\mu_{DRIFT} = \frac{L_{DRIFT}}{qN_{DRIFT} \cdot Z \cdot W_{DRIFT} \left(R_{ON2} - \frac{L}{2q\mu_{ch} N_{CH} Z (a - W_{S2})}\right)} \cdot (20)$$

The accuracy of the model extraction depends strongly on an accurate knowledge of the channel geometry. The extracted values of mobilities in the drift and channel regions can deviate from real material characteristics, but the proposed parameter extraction procedure successfully accomplishes the main goal of matching an experimental static family of curves with the simulated characteristic in the linear region of operation.

In order to predict the device behavior in the full range of operational conditions, the present parameter extraction procedure can be extended with the goal to establish temperature dependences of mobility in the channel and drift regions. The proposed model for temperature-dependent mobility takes the form of the empirical expression (1). The first term in (1) represents the carrier mobility in the region with given carrier concentration $N_D$ at a 300 K temperature. Therefore, (1) can be rewritten as

$$\mu(T) = \mu_{300} \left(\frac{T}{300}\right)^{-x} \quad (21)$$

where $\mu_{300}$ is the mobility in the given region (channel or drift) extracted at room temperature using the previously described procedure based on experimental data. Extrapolation
Fig. 8. (a) Drift region carrier profile of normally on JFET. (b) C–V measurements of input capacitances of normally on JFET.

Parameter $x$ is calculated using values of the mobilities extracted from static characteristics at room temperature and at an elevated temperature $T_1$ of 375 K

$$x = -\frac{\ln \left( \frac{\mu(T_1)}{\mu(300)} \right)}{\ln \left( \frac{T_1}{300} \right)}.$$  \hspace{1cm} (22)

Fig. 6 shows a comparison of the mobilities in the drift and channel regions obtained from experimental static characteristics and mobilities predicted using (21) and (22).

IV. EXAMPLE OF PROCEDURE IMPLEMENTATION

The parameter extraction procedure is applied to both a normally off and a normally on JFET sample provided by SemiSouth. The extracted JFET parameters for the two devices, given in Table II, are plugged into the model described in Section II for validation. The model was implemented in MATLAB computing software.

The normally off JFET has been used to illustrate the proposed extraction procedure in Section III (see Figs. 2–6). For this JFET, Fig. 7 shows a comparison of the simulated (solid lines) and experimental (dots) static output characteristics measured at room temperature (300 K) and at 375 K.

Fig. 8 shows the measurement results for the normally on JFET required for parameter extraction. Simulated (solid lines) output characteristics of the normally on SiC JFET and experimental (dots) static characteristics measured at room temperature and at 375 K are shown in Fig. 9.

For both devices, the simulated $I$–$V$ curves are in very good agreement with the experimental characteristics in the linear region, which validates the proposed mobility extraction procedure. The matching of the modeled and experimental characteristics in the saturation region is a matter of model adjustment, considering the field dependence of mobility and some uncertainty in the geometrical parameters. The model was particularly sensitive to the value of channel half.
The proposed parameter extraction approach allows obtaining major material properties of the JFET: the carrier concentrations and carrier mobility in the channel and drift regions. The developed procedure includes the extraction of parameters used in a proposed empirical temperature-dependent mobility model. Separate extraction for the channel and drift region mobility models is proposed. The validation of the approach is done by comparing the experimental and simulated static results at room temperature and at 375 K for both normally off and normally on SiC JFETs. The simulated I–V curves are in very good agreement with the experimental characteristics in the linear region owing to the separately extracted drift region and channel region mobilities.

ACKNOWLEDGMENT

The authors would like to thank SemiSouth Laboratories, Inc., for providing the JFET sample used for model validation.

REFERENCES


Jerry L. Hudgins (S’79–M’85–SM’91–F’04) received the Ph.D. degree in electrical engineering from the University of Texas at Austin, Austin, TX, in 1985. He is currently the Chair of the Electrical Engineering Department, the Director of the Nebraska Wind Applications Center, and an Associate Director of the Wind Engineering and Research Center. He has been with the University of Nebraska–Lincoln, Lincoln, NE, previously, he was on the faculty at the University of South Carolina, Columbia, until 2004. He has published over 100 technical papers and book chapters concerning power semiconductor devices and engineering education and has worked with numerous industries.

Zhiyang Chen received the B.S. degree in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2000, and the M.S. degree from Huazhong University of Science and Technology, Wuhan, China, in 2002. He has been working toward the Ph.D. degree at the University of South Carolina, Columbia, since 2004. From 2003 to 2004, he was an Assistant Engineer with the Chinese Academy of Sciences. His work was there to design special power supplies for high energy physics application. His research area is modeling and simulation of semiconductor power devices.

Dr. Hudgins served as the President of the IEEE Power Electronics Society for the years of 1997 and 1998 and as the President of the IEEE Industry Applications Society for 2003.
H. Alan Mantooth (S’83–M’90–SM’97–F’09) received the B.S. (summa cum laude) and M.S. degrees in electrical engineering from the University of Arkansas (UA), Fayetteville, in 1985 and 1987, respectively, and the Ph.D. degree from the Georgia Institute of Technology, Atlanta, in 1990.

He joined Analog in 1990 where he focused on semiconductor device modeling and the research and development of HDL-based modeling tools and techniques. Aside from modeling, his interests include analog and mixed-signal IC design and power electronics. In 1998, he joined the faculty of the Department of Electrical Engineering, UA, where he has been a Full Professor in the Department since 2002. In 2003, he cofounded Lynguent, an EDA company focused on modeling and simulation tools. He established the National Center for Reliable Electric Power Transmission at the UA in 2005, for which he serves as the Director. In 2006, he was selected as the inaugural holder of the 21st Century Endowed Chair in Mixed-Signal IC Design and CAD. He has published over 150 refereed articles on modeling and IC design. He is a holder of patents on software architecture and algorithms for modeling tools and has others pending. He is a coauthor of the book *Modeling with an Analog Hardware Description Language* by Kluwer Academic Publishers.

David C. Sheridan received the B.S., M.S., and Ph.D. degrees in electrical engineering from Auburn University, Auburn, AL, in 1995, 2001, respectively.

From 2001 to 2006, he was with IBM Corporation, Burlington, VT, where he worked on device design in CMOS and SiGe BiCMOS technologies. Since 2006, he has been with SemiSouth Laboratories Inc., Starkville, MS, performing research and development of SiC-based power devices and related technology.

Jeff Casady (SM’02) received the Ph.D. degree in electrical engineering from Auburn University, Auburn, AL, and the B.S. and M.S. degrees in electrical engineering from the University of Missouri, Columbia.

He is a cofounder of SemiSouth, Starkville, MS, and has over 20 years of semiconductor experience, primarily in the design and development of SiC power switches. After cofounding SemiSouth in 2000, he served as the President and Chief Executive Officer from 2002–2007. Since 2007, he has served as the CTO and Vice-President of Business Development for SemiSouth and has served as a Member of the Board from its inception until present. From 1999 to 2003, he was a Mississippi State University Faculty Member working in SiC power transistor development. From 1996 to 1999, he worked for Northrop Grumman on key projects, including the development of high-frequency S-band and L-band SiC RF and power transistors for pulsed narrow-band high-power radar applications (both ground based and airborne). He also worked on various SiC power devices such as thyristors, MOS field-effect transistors, and diodes. He has published more than 75 papers and is the holder of six patents. He has coauthored three book chapters and numerous magazine articles.

Enrico Santi (S’90–M’94–SM’02) received the Dr. Ing. degree in electrical engineering from the University of Padua, Italy, in 1988, and the M.S. and Ph.D. degrees from California Institute of Technology, Pasadena, in 1989 and 1994, respectively.

He was a Senior Design Engineer with TESLACO from 1993 to 1998, where he was responsible for the development of various switching power supplies for commercial applications. Since 1998, he has been with the University of South Carolina, Columbia, where he is currently an Associate Professor in the Electrical Engineering Department. He has published over 100 papers in power electronics and modeling and simulation in international journals and conference proceedings and is the holder of two patents. His research interests include switched-mode power converters, advanced modeling and simulation of power systems, modeling and simulation of semiconductor power devices, and control of power electronics systems.
AUTHOR QUERIES

AUTHOR PLEASE ANSWER ALL QUERIES

AQ1 = This sentence was rephrased for clarity. Please check if the original thought was retained, and correct if necessary.
AQ2 = This sentence was rephrased for clarity. Please check if the original thought was retained, and correct if necessary.
AQ3 = This sentence was rephrased. Please check if the original thought was retained, and correct if necessary.
AQ4 = “USC” is defined as “University of South Carolina.” Please check if appropriate, and correct if necessary.
AQ5 = “Bachelor degree” was changed to “B.S. degree.” Please check if appropriate, and correct if necessary.
AQ6 = “University of South” was changed to “University of South Carolina, Columbia.” Please check if appropriate, and correct if necessary.
AQ7 = “UA” is defined as “University of Arkansas.” Please check if appropriate, and correct if necessary.
AQ8 = Please provide the expanded form of “HDL.”
AQ9 = Please provide the expanded form of “EDA.”
AQ10 = Please provide the expanded form of “CAD.”
AQ11 = “CEO” was expanded as “Chief Executive Officer.” Please check if appropriate, and correct if necessary.
AQ12 = Please provide the expanded form of “CTO.”
AQ13 = “VP” was expanded as “Vice-President.” Please check if appropriate, and correct if necessary.
AQ14 = Please provide the specific location of the University of Padua.
AQ15 = “Caltech” was expanded as “California Institute of Technology.” Please check if appropriate, and correct if necessary.

END OF ALL QUERIES