An Interface for Switching Signals and a New Real-time Testing Platform for Accurate Hardware-in-the-Loop Simulation

Hernán P. Figueroa, Student Member, IEEE, Antonello Monti, Senior Member, IEEE, and Xin Wu, Student Member, IEEE

Hernán P. Figueroa, Antonello Monti, Xin Wu Department of Electrical Engineering, University of South Carolina, Columbia, SC, USA, e-mail: (figueroh, monti, wu6)@ieee.org

Abstract—Testing digital control systems for power electronics applications is an intricate procedure. An effective tool for the evaluation of electric systems and drives is provided by real-time Hardware-in-the-Loop (HIL) simulation, which is being increasingly used in industrial applications. However, to be practical, the real-time simulation platform must be inexpensive and easy to set up for various tests. In this paper, Virtual Test Bed (VTB) and its real-time extension (RTVTB), in conjunction with a custom hardware interface, are utilized to implement an affordable and versatile real-time testing platform for digital controllers. The hardware interface addresses the timing issues introduced by the presence of switching circuits in the system under test. Integrating the switching gate control signal, which comes from the hardware digital controller, requires very high time resolution. However, such high resolution is not necessary to accurately simulate the electric system under control. The proposed hardware interface separates the hardware requirements from the real-time simulation requirements in terms of time resolution, maintaining appropriate accuracy in the testing procedure.

Index Terms—Real-time simulation, Hardware-in-the-Loop, mixed-signal solver, averaging models, PWM signals.

I. INTRODUCTION

In general, testing digital control systems is a challenging procedure. Testing control systems for power electronics applications further complicates the operation, particularly because it frequently involves coupling the system with switching circuits. An effective tool for the evaluation of electric systems and drives is provided by real-time Hardware-in-the-Loop (HIL) simulation, which is being used increasingly in industrial applications, because it makes the testing of any new equipment safer and more reliable. Currently, extensive research is being carried out in academia and industry to apply real-time and HIL concepts in the development of suitable real-time simulation platforms [1][2][3]. However, many of the available commercial tools are costly and use complicated proprietary hardware.

The design and implementation of a real-time testing platform for power electronics equipment is becoming critical for industrial applications. In order to be practical, the real-time simulation platform must be easy to set up for various tests. Although it is possible to achieve a very fast simulation process by optimizing the code for a specific circuit, this approach precludes easy and quick specification of the topology of the system under analysis. In contrast, a platform using standard software enables the user to specify and change the topology rapidly, without compromising the speed of the simulation.

An additional problem for testing control systems is the cost of necessary equipment. During Hardware-in-the-Loop simulation, timing issues arise in the hardware-software interface, due to the presence of switching circuits in the system under test. The integration of the switching gate control signal, which comes from the hardware digital controller, requires the highest time resolution in the simulation. However, achieving this resolution is prohibitively expensive and time consuming for simulation of complex and dynamic models. To address this issue, a hardware interface is desirable in the simulation platform to separate the hardware requirements from the real-time simulation requirements in terms of time resolution, since high time resolution is not necessary to accurately simulate the electric system under control.

In this paper, Virtual Test Bed (VTB) [4] and its real-time extension (RTVTB) [5][6], in conjunction with a custom hardware interface, are utilized to implement an affordable and versatile real-time testing platform for digital controllers. The proposed hardware interface is implemented using a PIC microcontroller, providing an inexpensive means of accurately simulating switching components in HIL testing. This platform will allow engineers in any field to safely design and test very complex systems, substituting virtual models for critical components, thus reducing the risk, the cost and the time consumption of the final hardware testing process. The software and hardware structure of the proposed platform are described in detail and an application example is discussed.

II. SIMULATION ENVIRONMENT

The simulation environment is composed of the VTB and RTVTB. For both, the Signal Extension Resistive Companion solver (SRC) is currently implemented as the main core solver [4]. The description of these elements is detailed below.

A. Virtual Test Bed (VTB)

VTB is a new environment for design, analysis, and virtual prototyping of multidisciplinary systems. Currently,
VTB provides the ability to import dynamic models from a variety of environments (while enforcing data, signal, or natural coupling laws), to import structural models that describe the physical properties of a system, to create and drive advanced visualizations from within the simulation environment and to couple hardware and software naturally within the simulation system [7].

B. Signal Extension Resistive Companion (SRC) solver

The SRC solver is a mixed-signal solver based on the resistive companion method (RCM). An important feature of this solver is the support of signal coupling, which enables natural coupling between hardware and software and offers the possibility to perform HIL simulations. Detailed information can be found in [4].

C. Real-time Virtual Test Bed (RTVTB)

In this work, the real-time extension of VTB is adopted as the simulation environment for real-time HIL simulations. Being an adaptation of the Linux version of VTB, RTVTB shares the major parts of its architecture with the Windows version of VTB; this makes it convenient to export simulation models from the non-real-time platform to the real-time one. To extend the possibility of the VTB to real-time applications, the Real-Time Application Interface (RTAI) [8] is utilized. This open-source software, developed at the Politecnico di Milano, is used to create the hard real-time tasks that RTVTB needs to become a hard real-time Linux simulation environment.

Because of the features of the SRC solver, RTVTB can perform hard real-time HIL simulations, increasing the realism of the simulation and providing access to hardware features currently not available in software-only simulation models [9]. A more detailed description of RTVTB can be found in [5].

III. INTERFACE FOR SIGNAL AVERAGING

Complex power electronics systems are characterized by a combination of subsystems working at different time scales and with different needs in terms of time resolution. The fastest subsystem in the simulated system is the gate drive control subsystem. Its requirements in terms of time resolution depend on the switching frequency of the gate firing signal. A simple table can show how the different time resolutions affect the accuracy of the acquisition of the switching input signal coming from the hardware controller.

Table 1 shows that a time-step of 50 µs, which is more than acceptable from the system solution standpoint (being the value of the eigenvalues of a typical electrical system), is limited to an accuracy of 5%. Moreover, this can be considered a best case scenario, since it represents the error in the input evaluation stage and is likely to be amplified by the simulation process.

<table>
<thead>
<tr>
<th>Switching frequency</th>
<th>Timing resolution</th>
<th>Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 kHz</td>
<td>50 µs</td>
<td>10%</td>
</tr>
<tr>
<td>1 kHz</td>
<td>50 µs</td>
<td>5%</td>
</tr>
<tr>
<td>2 kHz</td>
<td>0.5 µs</td>
<td>0.1%</td>
</tr>
</tbody>
</table>

In order to address this issue, the separation of the hardware requirements for the real-time operation from the software requirements has been proposed [10]. This separation can be obtained by introducing a suitable hardware interface able to catch the commutation event of the switching signal with an accuracy higher than the one possible with a simple software structure; thus, the gated integration is performed on the simulation step while maintaining an appropriate accuracy.

A numerical simulation of a system composed of a buck converter connected to a resistive-inductive load can show this situation. The schematic of the example is shown in Fig. 1, where the circuit elements have the values $V_{DC} = 20\text{V}$, $R = 0.2\Omega$ and $L = 0.001\text{H}$.

Assuming an ideal buck converter, the differential equation of the system is as follows:

$$V_{DC} \delta(t) = R i_{L(t)} + L \dot{i}_{L(t)}$$

$$i_{L(t)} = \frac{R}{L} \int i_{L(t)} \, dt + V_{DC} \int \delta(t) \, dt$$

Let us consider the system input $\delta(t)$ as a firing signal with switching frequency of 2 KHz and duty cycle of 0.25. A software time resolution of 50 µs gives ten points for each switching cycle, which is sufficient to reasonably estimate the current ripple, but has a limited accuracy of 10% in the evaluation of the switching event. To minimize error, a hardware device with a time resolution of 0.5 µs is inserted into the hardware-software interface. In this way, the simulation accuracy is improved to 0.1% because it is now limited by the hardware interface capability and not by the simulation time step.

![Fig. 1 Schematic of the example system. A buck converter connected to an R-L load.](image.png)
Fig. 2 Acquisition of the PWM input signal $\delta(t)$. The simulation process receives input signal $\delta_1(t)$ when applying the software-only approach, or input signal $\delta_2(t)$ when using the custom hardware interface.

Fig. 2 shows how input $\delta(t)$ is acquired by the simulation platform. Using the software-only approach, signal $\delta_1(t)$ is obtained; on the other hand, the proposed custom hardware interface yields signal $\delta_2(t)$. At the time step where the switching event occurs, 50% of the signal input information is lost by $\delta_1(t)$, because the signal is considered “on” during the entire time step. In contrast, $\delta_2(t)$ maintains the input data for the integration process by introducing an average duty value of 0.5 at this simulation step.

Using these inputs, equation (1) is integrated, applying the runge-kutta order2 integration method, as formulated in equation (2).

$$i_{L(k+1)} = i_{L(k)} + \frac{h}{2} [f_1 + f_2 + h f_1, \delta_1(k)]$$

where:

$$f_1(x,u) = \frac{1}{L} \frac{d}{dt} x + V_{DC} u$$

$$f_2 = f(i_{L(k)}, \delta_2(k))$$

The simulated currents, $i_{L1}(t)$ and $i_{L2}(t)$, are presented in Fig. 3.

In this example, the value of the steady-state average current $i_{L2}(t)$ is expected to be 25 A, as is accurately estimated when using the proposed interface in the simulation. However, applying the standard software-only approach, the calculated current reaches 30 A at steady-state. In effect, the 10% accuracy of the input signal acquisition yields a total error of about 20% in the steady-state.

For the proof-of-concept of this approach, a PIC18F1320 microcontroller has been chosen. This very low cost device, with a resolution of 0.5 $\mu$s, has been programmed to receive a 2 KHz PWM input signal and to output an 8-bit value of the averaged duty every 50 $\mu$s. Inside the simulation software, an external interface model is created, to allow communication between the hardware interface and the RTVTB simulation environment. Fig. 4 depicts the structure of the interface.

Fig. 3 Calculated currents $i_{L1}(t)$ and $i_{L2}(t)$ using input signals $\delta_1(t)$ and $\delta_1(t)$ respectively.

IV. SIGNAL AVERAGED MODEL

Every power converter can be described by an averaged model. As an example, an averaged model for a single leg of a power inverter has been built. This model is used as a buck converter in the simulation example. The model considers the effects of turn-off dead time and difference in power losses between on and off states of the switches. Here we assume that the turn-on resistances of the switches have fixed values.

The circuit of a single leg of an inverter and its equivalent circuit, which uses a controlled voltage source, are shown in Fig. 5, where $\delta$ is the duty ratio and $R_{eq}$ is the equivalent power loss resistance. The representation of the model in a resistive companion form is presented in equation (3).
Considering the switching off dead time of the isolated gate bipolar transistor (IGBT), the duty ratio is modified as follows.

\[
\delta = \begin{cases} 
\delta_{in} - dt & |I_{out}| > 0 \\
\delta_{in} + dt & |I_{out}| \leq 0 
\end{cases}
\]

Where \(\delta_{in}\) is the input duty ratio, and \(dt\) is the switching-off dead time of the IGBTs. Considering the power loss, we have:

\[
R_{eq} = \begin{cases} 
R_s (\delta + R_d (1-\delta)) & |I_{out}| > 0 \\
R_s (1-\delta) + R_d \delta & |I_{out}| \leq 0 
\end{cases}
\]

Where \(R_s\) is the switch-on resistance of the IGBT, and \(R_d\) is the switch-on resistance of the diode.

V. EXPERIMENTAL RESULTS

Since the VTB Schematic Editor (SE) has not yet been implemented in Linux VTB, the schematic of the system is created and modified using the VTB SE on a Windows platform, as depicted in Fig. 6.

Non-real-time software simulations under Windows VTB are performed to verify the numerical results presented above; here a 0.25 duty PWM input signal and time steps of 50 \(\mu\)s and 0.5 \(\mu\)s are used to calculate the current passing through the induction load. The resulting currents are displayed in Fig. 7.

The waveform of the simulation with 50 \(\mu\)s time step yields a steady-state value of \(-30\) A (29.4 A), this is due to the 50\% data loss at the time step when the switching event occurs (the input is considered permanently on during this time step). However, when using 0.5 \(\mu\)s time step, the expected steady-state value of \(-25\) A (24.5 A) is computed. As it can be observed, there is a slight difference between the calculated current values from the VTB simulation and the numerical analysis above, because the non-ideal internal resistance of the system models.

The system is then exported into a Dell Precision\textsuperscript{TM} Workstation 450n Linux machine for the execution of its real-time HIL simulation. This computer, featuring RTVTB, has two 2.66GHz Intel\textsuperscript{®} Xeon\textsuperscript{™} Processors and 512MB RAM. However, only one processor is used in this experiment.

The simulation real-time clock is set to 50 \(\mu\)s. The simulation process communicates with the real world through an external interface model. Employing comedi Linux drivers [11], this model is able to access the digital and analog channels of a commercial data acquisition card (Advantech PCI-1710). In this experiment, the external interface is used to output waveforms from the simulation environment to a scope and to allow interaction between RTVTB and the signal averaging hardware interface.

The hardware interface is implemented, as described above, in a PIC controller. An 8-bit digital output port of the PIC18F8720 chip is connected to the 8 least significant bits of the digital input port of the Advantech PCI-1710 acquisition device. A PWM signal, with a fixed duty cycle of 0.25, is then applied to an input channel of the PIC controller.
Every time step, the PIC microcontroller outputs the average duty value of the switching signal, proportional to the percentage of the time the signal is “on” during this time step; inside the simulation, the external interface receives and scales this value from 0 to 1. An example of the resulting average duty signal is presented in Fig. 7. The synchronization between the real-time simulation process and the hardware interface is achieved by an interrupt signal, sent from the Linux machine to the microcontroller to request the new average duty value.

The resulting current waveform is presented in Fig. 9. It has been rescaled using a scaling factor of 1/10 due to the voltage range limitation of the data acquisition card. As can be observed, the steady-state current is 24.6 A (2.46 V on the scope), which is the expected value from the non-real-time simulation.

The averaged value of the current and its switching harmonic content are accurately simulated using a 50 µs time step, thus effectiveness of the proposed hardware interface its demonstrated.

VI. CONCLUSIONS

A reliable real-time platform for accurate HIL simulation has been implemented using RTVTB as the simulation environment. The high accuracy of the approach proposed in this paper has been successfully verified by the development and realization of an inexpensive hardware interface. In addition, a new definition of switching function based on averaged duty values has been proven to be accurate on the final waveform reconstruction.

A detailed analysis of the effect of the input switching signal evaluation on the total simulation error has also been presented, through numerical and experimental examples.

In the future, the proposed hardware will be designed with FPGA technology to improve the configurability of the interface. Another possibility is to use the same concept to recreate realistic feedback from the simulation process to the digital control system, such as the speed-position digital signal of a sensor encoder. The FPGA-based interface can be extended to address this problem with hardware, without overloading the simulation platform.

VII. ACKNOWLEDGEMENTS

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VIII. REFERENCES