Temperature Effects on IGCT Performance

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Abstract – The Integrated Gate-Commutated Thyristor (IGCT) is an advanced semiconductor device for high frequency, high power applications. This work presents a detailed discussion of experimental dynamic characteristics of IGCTs at ambient temperatures ranging from –40°C to 50°C. A lumped-charge physics-based IGCT model with full temperature response is also developed in this work. A chopper circuit with an inductive load is employed to test the IGCT switching behavior both experimentally and by simulation. Comparison between the experimental and simulation results is made and discrepancies are discussed.

I. INTRODUCTION

The Integrated Gate-Commutated Thyristor (IGCT) consists of an integrated gate board and a Gate Commutated Thyristor (GCT). An anti-parallel diode is also integrated in the reverse conducting IGCT. The IGCT is an advanced semiconductor switch for high frequency, high power applications above 100 kW. It satisfies the conflicting demands of high current, high voltage and fast turn-off through carrier lifetime engineering on the one hand, and the flexible functionality of a standard gate unit on the other [1]. Since 1997, when it was first commercially introduced, the IGCT has rapidly gained acceptance in major areas of high power electronics, such as propulsion inverters for mass transit and locomotives, high power industrial drives for steel and paper mills, and utility power conditioning, including static VAR compensation and flexible AC transmission [2].

It is of interest to study the dynamic and static properties of IGCTs over a wide range of operating temperatures because they are expected to be used in power applications with junction temperature extremes ranging from –40 to 125 °C, and the associated ambient operation temperature ranging from -40 to 60 °C. The temperature related information provided by semiconductor manufactures is limited; it normally includes voltage drop and energy loss at 115 °C or 125 °C. There has been considerable information introducing the advantages of IGCTs [1-4], but little or no literature reports concerning the behavior, especially the switching characteristics of IGCTs over a wide temperature regime.

In this work, we will present a detailed discussion of experimental dynamic characteristics of IGCTs at ambient temperatures ranging from –40 to 50 °C. A chopper circuit with an inductive load is employed to test the IGCT switching behavior. There is no turn-off snubber included in the circuit, so that we can test the hard switching characteristics of the device.

Besides the experiment, a lumped-charge physics-based IGCT model with full temperature response is also developed in this work. Some important physical effects, such as Auger recombination, are considered in this model. In addition to the power switch, a simplified gate drive is integrated into the IGCT model. Comparisons between the experimental and simulation results are made and discrepancies are discussed. Some of the device characteristics at extremely high and low temperatures, which are difficult to test, are studied by simulation.

II. IGCT OPERATION PRINCIPLE

The key idea of the IGCT is the hybridization of an improved GTO structure and an extremely low-inductance gate drive. In the conducting state, the IGCT is a regenerative thyristor switch like a SCR or GTO. As illustrated in Fig.1 (left), the IGCT is characterized by a high current capability and a low on-state voltage. In the beginning of turn-off, the gate-cathode junction is reverse-biased and the cathode emitter is turned off before the voltage at the main blocking junction rises, resulting in an extremely fast commutation of the cathode current to the gate. Thereafter, the device is turned off like a transistor, as shown in Fig.1 (right). Therefore, the IGCT operates on the principle that thyristors are suited as conduction devices whereas transistors are better as controlled turn-off devices [1].

Fig. 1. Conducting (left) and blocking (right) conditions for the IGCT.

III. ASYMMETRIC IGCT SEMICONDUCTOR TECHNOLOGY

Some advanced semiconductor technologies are employed in an IGCT, such as a punch through (PT) structure and a transparent anode.

There are two ways to achieve a high blocking voltage: by increasing the thickness of the N’ drift region in nonpunch-through (NPT) devices or applying the punch-through (PT) concept [5]. The PT IGCT is also called an asymmetric IGCT because its reverse blocking voltage is much lower than its
forward blocking voltage. In this work, our experiments and simulations are focused on the asymmetric IGCT.

The basic structure, doping profile and field distribution during the forward blocking state of an asymmetric IGCT device are shown in Fig. 2. The typical trapezoidal shape of the electrical field is achieved in the PT IGCT. The PT structure allows a rated blocking voltage to be achieved with a narrower N- base than the NPT design, and thus achieve a lower on-state voltage and lower switching losses. This buffer layer also causes a reduction in the injection efficiency of holes into the N$^-$ base, which in the design of the IGCT is a benefit for turn-off.

Transparent anode technology is adopted in the IGCT, as shown in Fig. 3. This makes the IGCT different from a conventional GTO with anode shorts. During the IGCT turn-off phase, electrons can be swept out across the anode emitter as if it were shorted, but without the inconvenience of shorts [6]. As a consequence, the gate sensitivity is increased and the turn-off loss is reduced.

IV. IGCT TESTING AND EXPERIMENTAL RESULTS

A. Test circuit and measured switching waveforms

An inductive load circuit, as shown in Fig. 4, was built to test the switching characteristics of the IGCT. $L_{cl}$ represents a parasitic inductance; $L_{Load}$ is the large inductive load. A turn-on snubber consisting of $L_i$ (25 µH), $R_s$ (4.2 Ω) and $D_1$ was designed to limit the IGCT turn-on $di/dt$. The control signal is galvanically isolated from the gate board. The IGCT is placed into a chamber in which the temperature can be controlled. The maximum ratings of the test device are given in Table 1.

![Fig. 2. Structure, doping profile and electric field distribution during forward blocking of an asymmetric IGCT.](image)

![Fig. 3. Charge extraction for a conventional GTO and with a transparent anode (as in the IGCT).](image)

![Fig. 4. Circuit for testing IGCT switching.](image)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Max. Rating</th>
<th>Description</th>
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<tbody>
<tr>
<td>$V_{DRM}$</td>
<td>4500 V</td>
<td>Repetitive peak off-state voltage</td>
</tr>
<tr>
<td>$I_{TQHM}$</td>
<td>340 A</td>
<td>Max controllable turn-off current</td>
</tr>
<tr>
<td>$V_{DClink}$</td>
<td>2800 V</td>
<td>Permanent DC voltage</td>
</tr>
<tr>
<td>$I_{TSM}$</td>
<td>2100 A</td>
<td>Max peak non-repetitive surge current</td>
</tr>
</tbody>
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Table 1. IGCT Maximum Ratings

A set of experimental switching waveforms for the IGCT was obtained as shown in Fig. 5. The upper waveforms show the anode voltage and current; the lower waveforms show the gate information -- control signal, gate voltage, and gate current. A 4 µs delay can be observed before the device responds to the control signal. The $di/dt$ during the turn-off indicates that about 300 nH of insertion inductance was introduced by the measuring device. The large parasitic gate inductance greatly delayed the turn-off process, and negatively affected the function of the integrated gate-drive. To eliminate the effect of this parasitic gate inductance, the gate current was not measured for other experiments in this work.

One of the important pieces of information given by Fig. 5 is that the storage time ($t_s$) is much shorter than that of a typical GTO. The storage time is the time delay between the application of the reverse gate current and a decrease in the anode current. The waveforms indicate a 1.7 µs storage time. Further measurements indicated that the $t_s$ was only 0.5 µs to 0.6 µs if the gate inductance was limited.

During the storage phase, the gate current extracts charges from the P-base region until the PN junction becomes reverse biased. The $t_s$ is determined by turn-off gain ($I_G/I_0$), high level lifetime ($\tau_{HL}$) and base widths ($W_{BP}$, $W_{BN}$) as given by (1), [9].

$$t_s = \left(1 - \frac{I_0}{I_G}\right) \times \frac{\tau_{HL} \times W_{BP}}{W_{BP} + W_{BN}}$$ (1)

In an IGCT, the unity turn-off gain reduces the $t_s$ to near zero, which provides the possibility for IGCTs to work at high frequencies.
B. Turn-off characteristics and temperature effects

In the turn-off phase the IGCT behaves like an open base PNP transistor because the emitter junction is turned off prior to the main blocking voltage rise. Therefore, no external dv/dt limitation is required, which means no turn-off snubber is required.

An experimental turn-off waveform is shown in Fig. 6. The turn-off time is about 3.5 \( \mu s \) with a conducting peak current of 300 A and blocking voltage of 2500 V. It shows typical hard turn-off characteristics. The voltage increases rapidly after the storage phase and the dv/dt reaches 5000 V/\( \mu s \).

The IGCT turn-off process occurs in three phases. The first phase is the storage phase, described previously, which could be ignored. In the second phase, the depletion layer across the center junction expands in the N-base region to support the increasing anode voltage, and sweeps out stored charge from the N-base. This phase ends when the anode voltage reaches its steady state value. Thereafter, the remaining charge in the N-base is removed by recombination, the third phase.

The time interval for the second phase is proportional to the high-level lifetime \( \tau_{HL} \):

\[
\tau_{HL} = \tau_{\rho 0} \times (1 + \zeta) \tag{2}
\]

Where, \( \tau_{\rho 0} \) is the minority carrier lifetime in N-base region, and \( \zeta \) is the hole to electron capture cross-section ratio. \( \tau_{HL} \) is weakly dependent on temperature \([9]\). The time interval for the third phase is determined by the low-level lifetime \( \tau_{LL} \):

\[
\tau_{LL} = \tau_{\rho 0} \times \left(1 + e^{(E_r - E_i)/kT}\right) + \tau_{\rho 0} \times \zeta \times e^{(2E_r - E_i)/kT} \tag{3}
\]

Where \( E_r \), \( E_i \) and \( E_F \) are the energy positions of the recombination center, intrinsic Fermi level, and N-base Fermi level, respectively. Because the exponential terms in (3) are negative, \( \tau_{LL} \) increases with temperature over the tested temperature range.

Two experimental turn-off current families at various temperatures are shown in Fig. 7. In both current families, the time interval for the second phase changes little with the temperature. However, the current tail increases noticeably as the temperature increases. This different response to the temperature is because the two phases are determined by different lifetime as mentioned above.

Fig. 8 shows turn-off energy losses \( E_{\text{off}} \), as function of temperature. It can be seen for each conduction current value \( E_{\text{off}} \) increases as the temperature increases. It should be noted that at the highest value of anode current (300 A), the temperature dependency is more pronounced. This is due to the compounding effects of increased stored base charge at high currents and the increasing carrier lifetime as the temperature rises.
Fig. 7. Anode currents during turn-off at temperatures from –40 to 50 °C. The conduction currents are (a) 200A, and (b) 300A.

Fig. 8. Turn-off loss vs. temperature for three current values.

V. LUMPED-CHARGE IGCT MODEL WITH FULL TEMPERATURE FEATURES

A. Model description

This Level-2 physics-based IGCT model is developed by employing the lumped-charge modeling technique, which reduces the complexity while retaining the internal carrier transport processes and basic structural information of the device [7].

As shown in Fig. 9, based on the lumped-charge modeling technique, 11 nodes are selected for the IGCT, in which node 0, 1, 3, 4, 6, 7, 9 and 10 are connection nodes, while nodes 2, 5 and 8 are charge storage nodes. The connection nodes are located at the boundaries of depletion regions, and the charge storage nodes are located in the centers of undepleted regions of the N buffer layer, N⁺ base, and P base. All the current components can be expressed by the lumped hole and electron charge values at the nodes, the transit times of holes and electrons, and the voltage drops between adjacent nodes. The basic equations are adapted from a GTO model in reference [8]. However, for an asymmetric IGCT, a buffer layer is embedded, making the IGCT semiconductor structure different from that of the GTO modeled in [8]. Also, a gate drive is integrated which makes the device behave similarly to that of a digitally controlled switch. The above mentioned important new features of the IGCT are captured in this model. Furthermore, some important physical effects, which affect the behavior of the device but were not included in the GTO model, are considered in this IGCT model, such as Auger recombination and material thermal dependencies. The equations caused by the embedded buffer layer can be derived similarly as in reference [8]. Other new features mentioned above are described below.

(1) Auger recombination

Auger recombination reduces the lifetime notably for high carrier densities above $10^{17}$ cm⁻³, which is quite possible for an IGCT device. In order to simulate the turn-off transient accurately, an expression for the lifetime that includes the Auger effect is adopted in this model and given by (4). $C_{aug}$ is the Auger recombination coefficient in units of cm⁶·s. As a result, the carrier lifetimes in the N-base and P-base regions are carrier density dependent.

$$\tau = \left(\frac{1}{\tau_0} + \frac{1}{C_{aug} \times p^2}\right)^{-1}$$

(4)
(2) Thermal effect

The junction temperature of the device is estimated by the thermal equivalent circuit shown in Fig. 10. The power input source (current source) can be expressed by equation (5). The R and C values are based on data sheet parameters or on package physical parameters and constants (e.g. thermal conductivity and heat capacity of the materials). Most of the semiconductor parameters are temperature dependent and will affect the device behavior. The main parameters, such as intrinsic concentration, mobility, and lifetime, have temperature relationships presented by (6) to (9), as described in reference [9]. These parameters are used to calculate the transit times, excess carrier concentration, junction built-in potential, and saturation current.

\[ P_{Si} = i_a \times V_{AK} + i_{Gon} \times V_{GK} \]  

(5)

\[ n_i = 3.87 \times 10^{16} \times T^{3/2} \times \exp(-7.02 \times 10^{3} / T) \]  

(6)

\[ \mu_e = 1360 \times (T / 300)^{2.42} \]  

(7)

\[ \mu_p = 495 \times (T / 300)^{2.2} \]  

(8)

\[ \tau = \tau_0 \times \exp(T / 300)^{3/5} \]  

(9)

Fig. 10. Coupled thermal equivalent circuit used to calculate the junction temperature.

(3) Integrated gate

The integrated gate drive is simply presented by a signal (voltage) controlled voltage source and a signal (voltage) controlled resistor. The logic is:

If \( CS = \text{on} \rightarrow \begin{cases} V_{Gapp} = V_{G\text{ max}} \\ R_G = R_{G\text{ min}} + R_{G\text{ max}} \left( 1 - \exp\left( -1/\tau_c \right) \right) \end{cases} \)

If \( CS = \text{off} \rightarrow \begin{cases} V_{Gapp} = -V_{G\text{ max}} \\ R_G = R_{G\text{ off}} \end{cases} \)

Where CS is the control signal. This simplified gate drive ensures that the IGCT is turned on during a short time period and is turned off with a unity turn-off gain.

B. Simulation results

The IGCT model is implemented using Matlab. An inductive load chopper circuit similar to Fig. 4, without a turn-on snubber, is adopted to verify the IGCT model. For simulation purposes the load inductance is substituted with an ideal current source. Figs. 11 to 13 present some of the simulation results.
Fig. 11 is one of the sets of simulated anode switching waveforms during hard switching. The anode current and gate current waveforms during turn-off are shown in Fig. 12 and indicate unity turn-off gain in the presented IGCT model. Fig. 13 presents a family of anode current turn-off waveforms at various junction temperatures and indicates appropriate behavior as the temperature changes.

VI. COMPARISON BETWEEN EXPERIMENTAL DATA AND SIMULATION RESULTS

A comparison between simulation and experimental turn-off current is shown in Fig. 14. A slightly slower anode current fall time is observed in the simulation result as compared to the experimental waveform. This is because different lifetimes for high- and low-level injection were not used. The transparent anode was also not considered in this model, which would have caused a longer current tail in the simulation.

Fig. 14. Experiment and simulated anode current turn-off waveforms.

Fig. 15 shows the energy loss vs. turn-off current at various temperatures. The simulated energy losses are a slightly higher than, but close to the experimental results. The higher energy loss indicated by simulation is expected, because the transparent emitter was not considered in this model. As mentioned above, the transparent anode emitter reduces the turn-off time and corresponding energy loss.

VII. CONCLUSION

The IGCT switching characteristics were studied at temperatures from –40 to 50 °C. It has been shown that the IGCT has a hard switching capability over the experimental temperature range. The anode current fall speed in the turn-off process is weakly dependent on temperature, and the current tail increases noticeably as the temperature increases. The turn-off energy losses correspondingly increase with temperature, with the temperature dependency becoming more pronounced at higher current values. A lumped-charge physics-based IGCT model with full temperature response was developed to simulate the device characteristics at extremely high and low temperatures, where testing of the device due to its integrated gate drive, makes it difficult. The model was shown to give very good agreement with experimental waveforms and correctly modeled the behavior under changing temperatures. To model the IGCT precisely, the transparent anode should be considered and different lifetimes should be used for high- and low-level injection.

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