Multi-Resolution Modeling of Power Converter Using Waveform Reconstruction

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Abstract

Computer simulation of switching power converters is complicated by the discontinuous (switching) nature of the converter waveforms. When switching details of the waveforms are of interest, detailed simulations requiring extremely small time steps are needed. On the other hand, so-called averaged models allow capture of low-frequency converter dynamics (of interest for example when closing the feedback loop) by computing averaged continuous waveforms. The possibility of using relatively large time steps makes averaged models computationally efficient. A real-time hierarchical approach that combines the advantages of the two methods is proposed. An averaged model and a detailed model are used alternately in successive time intervals. The final state of one model at the end of a time interval is used to calculate the initial conditions for the other model running in the following time interval. The method is illustrated with a buck converter. The combined use of two models with a hierarchical or multilevel approach is shown to provide a powerful simulation tool for analysis and design. The detailed model is used 10% of the time and the averaged model 90% of the time. Results indicate that the detailed behavior is accurately simulated when the detailed model runs, and the overall simulation time cost is lowered by running the averaged model 90% of the time. This approach provides a way to simulate the detailed behavior of a specific part in a rather large switching circuit network.

1. Introduction

Simulation plays an important role in the analysis and design of power-electronic circuits [1]. This involves several analytical and computer-based approaches including detailed circuit analysis with device models [6], state-space averaging and circuit-based averaging [2-3,6], piecewise linear switched-circuit simulators [6], use of control-oriented system solvers [4-6] and sampled-data modeling approaches [6]. Each of these approaches has advantages and limitations that make it suitable for some but not all simulation problems associated with a power electronic circuit. Hence, it is not advisable to answer all questions at once in one simulation.

As an example of the problems encountered, consider that electronic power converters are most easily described in terms of the circuit topology and the control algorithm for switching, while the motor (and its mechanical load) powered by the converter may be described by differential equations formulated in terms of state variables. The dynamics of the electronic power converter are fast while the dynamics of the mechanical components are quite slow. Full analysis of the problem requires a simulation to cover a large time span to capture the slow dynamics but with a small time step dictated by the fast dynamics. A small time step is especially necessary to compute switching times with adequate resolution to ensure accuracy of the voltage, and the problem is exacerbated at high switching frequencies. All of these considerations lead to a large number of time-steps in such simulations, and hence a lengthy wait for simulation results.

One approach to minimizing the execution time is to use variable time steps. However, in order to capture any details in the switching waveform, the time step must still be much smaller than one-half of the switching period. Hence, the simulation time cost is primarily dictated by the switching frequency.

An alternative approach is offered by the development of computer network techniques that lead to a distribution of the computing load. This offers a great potential for comprehensive simulation of power-electronic circuits using a hierarchical or multilevel approach [6-8] such as is implemented in the Virtual Test Bed (VTB) and described here. VTB is a computing environment that allows proof-testing of power system designs before hardware is actually assembled [11].

By adopting this multilevel approach the VTB can display the detailed switching waveform in an interactive oscilloscope-like view while the simulation proceeds at a high rate. This enables a highly interactive environment in which one can adjust system parameters, for instance, to

meet a particular ripple requirement, and immediately see the effect on system performance.

The real-time hierarchical approach described here exploits the power of network-oriented computing to:

1. Support both top-down (mission-oriented) and bottom-up (design-oriented) approaches.

2. Use different tools and techniques to study the circuit at various levels of detail. At the lower levels, circuits and devices are modeled in great detail; while at the higher levels, some details are ignored in order to capture only the dominant behavior of the module or system.

3. Preserve the value of existing models and existing modeling skills.

We will illustrate the benefits of the hierarchical method in this paper by application of the technique to simulation of a buck converter – a device that converts a relatively high voltage to a relatively lower voltage as necessary for whatever equipment it supplies. The converter is represented at two levels – the high-level model termed the State-Space Averaging Model (SSA) [2] and the detailed model termed the Switching Detail Model (SD). These two forms are often used in the simulation and analysis of power electronic circuits. For the SSA model a large time step can be adopted, not limited by the switching frequency, because the signal at switching frequency becomes time-averaged.

Thus the simulation time cost of the SSA model is low. The time step is decided by the frequency response of the time-invariant electrical network and is not directly related to the switching frequency. By definition these models correctly represent only the low-frequency time-average behavior.

Detailed simulations based on SD models are still necessary in order to examine the wide-bandwidth switching waveforms. Here, the time step *is* determined by the switching frequency, so SD simulations are computationally intensive. The simulation time cost rises with the switching frequency (higher switching frequencies are trend in power electronics). The difficulty is to reach a tradeoff between low simulation time cost and adequate resolution.

In this paper we describe a Hybrid model that was implemented by using the SSA model and SD alternatively as shown in Fig.1 and Fig.2, illustrates the tradeoff between the time cost of the two levels of detail, and the fraction of simulation time described by the two levels of detail. The Hybrid model uses the SSA model to compute the low-frequency behavior of the converter during the first 90% of each Hybrid model time interval and the SD model to compute the detailed time-domain behavior during the next 10% of the time interval. This method is implemented both in ACSL [9], a commercially available state–space based simulator, and in the VTB.

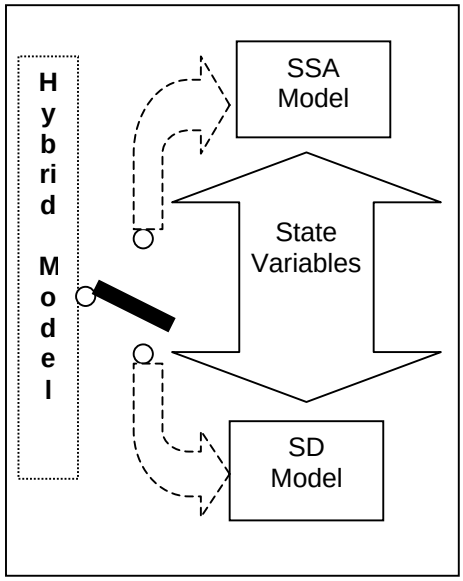

Fig.1 The SSA, SD and Hybrid models

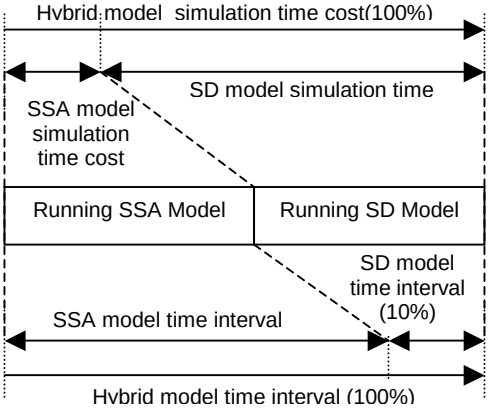

Fig.2 Simulation time cost and time interval in sub-model of the Hybrid model

Results indicate that the detailed switching behavior can be observed in the 10% of each Hybrid model time interval in which the SD model runs. Running 90% of each Hybrid Model Time Interval using the SSA model lowers the overall simulation time cost.

This hierarchical approach provides a way to simulate the detailed behavior of one component in a rather large switching network and substantially increases the capabilities of the present models. Although the hierarchical method may not eliminate the need for detailed system simulation in all cases, it does provide a computationally economical alternative for a variety of studies useful in the design and evaluation of electro-mechanical systems that include switching circuits.

2. Method

In this section, we first give the state equations for the SSA model, then for the SD model. Then we discuss the relationship between the state variables of the two models at the beginning of each time cycle. The choice of appropriate time cycle limits and conditions are also described.

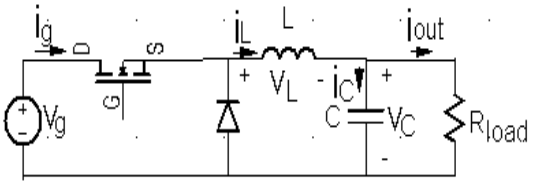

Fig.3 buck converter

Buck converter model

The buck converter is shown in Fig.3. For continuous mode operation, the input current waveform is as shown in Fig.4. The inductor voltage and current waveforms are shown in Fig.5, while the capacitor voltage and current waveforms are shown in Fig.6. In Fig. 4, Fig.5 and Fig.6, D is the fraction of the switching cycle T during which the switch is on, and D' is the fraction when the switch is off. These figures also identify terms used in the model definitions that follow

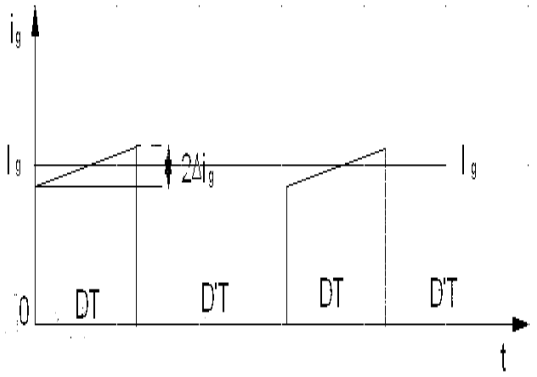

Fig.4 input current

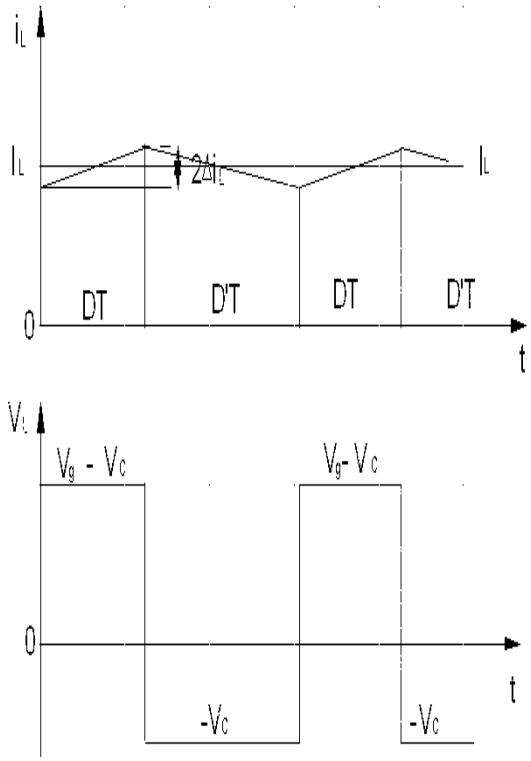

Fig.5 inductor current and voltage

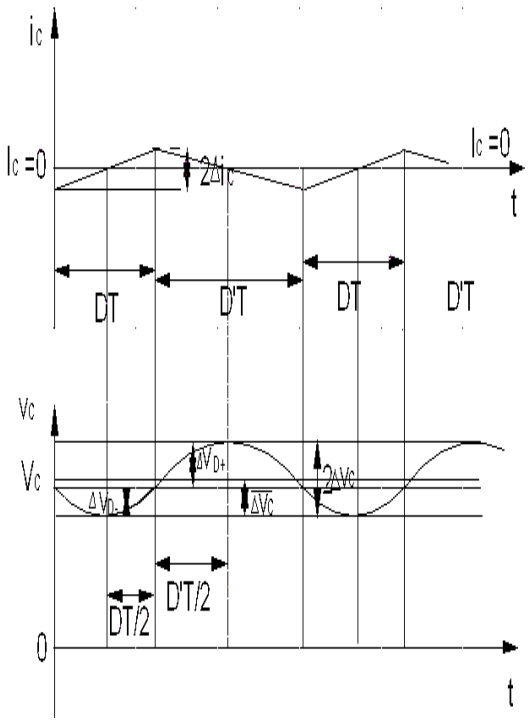

Fig.6 capacitor current and voltage

State variables

The state variables for this buck converter system are the inductor current i_L and the capacitor voltage v_C, which are defined by equations (1) that pertain to both the SSA and SD models.

$$\begin{cases} v_C(t) = \frac{1}{C}\int_0^t i_C dt + v_{C0} \\ i_L(t) = \frac{1}{L}\int_0^t v_L dt + i_{L0} \end{cases} \quad (1)$$

where i_{L0} and v_{C0} are initial values for inductor current and capacitor voltage, respectively.

State-space averaged model (SSA)

The DC component of inductor current and the DC component of capacitor voltage are the two state variables used in the state-space averaged model of the buck converter. The average state space equations of the buck converter are

$$\begin{cases} V_C(t) = \frac{1}{C}\int_0^t I_C dt + V_{C0} \\ I_L(t) = \frac{1}{L}\int_0^t V_L dt + I_{L0} \end{cases} \quad (2)$$

Here, V_{C0} and I_{L0} are initial values for inductor current and capacitor voltage, respectively. The average voltage impressed across the inductor is

$$V_L = DV_g - V_C \quad (3)$$

And the average current through the capacitor is

$$I_C = I_L - I_{out} = I_L - \frac{V_C}{R_{load}} \quad (4)$$

Substituting these expressions for V_L and I_C into equation (2), we get the SSA model:

$$\begin{cases} V_C(t) = \frac{1}{C}\int_0^t (I_L - \frac{V_C}{R_{load}})dt + V_{C0} \\ I_L(t) = \frac{1}{L}\int_0^t (DV_g - V_C)dt + I_{L0} \end{cases} \quad (5)$$

Switching Detail Model (SD)

The detailed state equations of the buck converter differ only slightly from the average state equations, and are expressed as

$$\begin{cases} v_C(t) = \frac{1}{C}\int_0^t (i_L - \frac{v_C}{R_{load}})dt + v_{C0} \\ i_L(t) = \begin{cases} \frac{1}{L}\int_0^t (v_g - v_C)dt + I_{L0}, \\ \text{when the switch is on;} \\ \frac{1}{L}\int_0^t (-v_C)dt + I_{L0}, \\ \text{when the switch is off.} \end{cases} \end{cases} \quad (6)$$

The inductor current ripple is estimated as

$$\Delta i_L = DT(V_g - V_C)/2L = D'TV_C/2L \quad (7)$$

As shown in Fig.6, the capacitor voltage increases during the time when the capacitor current is positive. This time interval can be divided into two parts. During the first part, the capacitor current starts from zero and increases to its peak value. Accordingly, the increase of the capacitor voltage can be estimated by

$$\Delta v_{D-} = \frac{\Delta i_C DT}{4C} \quad (8)$$

During the second part, the capacitor current starts at its peak and decreases to zero. During this time, the increase of the capacitor voltage can be estimated by

$$\Delta v_{D+} = \frac{\Delta i_C D'T}{4C} \quad (9)$$

Notice that Δv_{D-} and Δv_{D+} are in general different.
The average value of the capacitor voltage ripple is then

$$\overline{\Delta v_C} = \frac{\Delta i_C T}{C}\left(\frac{D^2}{12} + \frac{D'^2}{6} + \frac{DD'}{4}\right) \quad (10)$$

The derivation of equation (10) is listed in Appendix B.

Switching between the SSA and SD models

From Figs.5 and6, one can see that at the beginning of each cycle, the instantaneous value of the capacitor voltage is

$$v_C(nT) \approx V_C - \overline{\Delta v_C} + \Delta v_{D-}$$
$$= V_C + \frac{\Delta i_C T}{C}\left[\frac{D}{4} - \left(\frac{D^2}{12} + \frac{D'^2}{6} + \frac{DD'}{4}\right)\right] \quad (11)$$

Where n is an integer.

At the same time, the instantaneous value of the inductor current is

$$i_L(nT) = I_L(nT) - \Delta i_L \qquad (12)$$

Where Δi_L is defined in equation (7).

If the capacitor is big enough, its voltage has only a small ripple. Then the load current is nearly constant and the capacitor current ripple is approximately the same as the inductor current ripple:

$$\Delta i_C = \Delta i_L \qquad (13)$$

Substituting equation (13) into equation (11), we get

$$v_C(nT) \approx V_C + \frac{\Delta i_L T}{C}[\frac{D}{4} - (\frac{D^2}{12} + \frac{D'^2}{6} + \frac{DD'}{4})] \qquad (14)$$

Let us put equation (14) and equation (12) together. Note that nT in these two equations represents the exact time points when the switch turns on. Hence, for every few distinct cycles, the algorithm can swap from the SSA model to SD and adjust the two state variables, V_C and I_L, according to equations (12) and (14).

$$\begin{cases} v_C(nT) \approx V_C + \frac{\Delta i_L T}{C}[\frac{D}{4} - (\frac{D^2}{12} + \frac{D'^2}{6} + \frac{DD'}{4})] & (14) \\ i_L(nT) = I_L(nT) - \Delta i_L & (12) \end{cases}$$

When the algorithm swaps from SD to the SSA model, equations (15) and (16) that are derived from (12), (14) are used to adjust the two state variables, V_C and I_L.

$$\begin{cases} V_C \approx v_C(nT) - \frac{\Delta i_L T}{C}[\frac{D}{4} - (\frac{D^2}{12} + \frac{D'^2}{6} + \frac{DD'}{4})] & (15) \\ I_L = i_L(nT) + \Delta i_L & (16) \end{cases}$$

These results apply to a converter running not only open loop but also closed loop. The case of closed loop will be discussed in another paper.

Limitations and further work

The above derivations assume that the converter operates in continuous conduction mode (current through the inductor never falls to zero). Further work is necessary to extend the method to the discontinuous conduction mode.

3. Simulation example

Acuuracy

The Accuracy of this hierarchical approach is first demonstrated by a simulation written in ACSL [9] (Advanced Continuous Simulation Language). The converter is operated with open loop control, and performance in steady state and following a transient perturbation are shown as calculated by the SD, SSA, and Hybrid models.

Reference with to Fig.3, the circuit parameters are:

input voltage source V_g=950 V
switching frequency=20.0kHz
inductor L=160 μH
capacitor C=200.0μF
resistor R_{load}=4.0Ω

In the Hybrid model, the swapping period is 200 cycles of the switching converter (refer to Fig.2). For the first 90% of the 200 cycles (180 cycles) the simulation runs in SSA mode, and for the next 10% (20 cycles) it runs in SD mode.

The integration algorithm is second order Runge-Kutta with fixed time step. All the simulation result graphs are shown in Fig.7 to Fig.18 in Appendix A. Simulations were run under four different conditions that are described in detail below.

Steady state. Figures 7 through 9 show results for the SD, SSA and Hybrid models, respectively for the converter running in steady state with the output voltage set to 800 volts. The waveforms shown are of the output voltage and inductor current. In Fig.9, the Hybrid model runs in SSA mode during the first two time divisions and in SD mode during the last five time divisions. The time scale is 20 microseconds/division. Comparing the figures, we can see that the detailed waveform reconstructed by the Hybrid model is very similar to the corresponding waveforms obtained from SD model.

Step change of load. Figures 10, 11, and 12 show the response of output voltage and inductor current to a step change of the resistive load from 4 ohms to 6 ohms. The waveforms based on the SD, SSA and Hybrid models are shown. In Fig.12, the SSA sub-model runs during the first three time division and the SD sub-model runs during the following five time division. The time scale is 200 micro seconds/division; The dynamic response is much larger than the switching ripple. However, the Hybrid model still

successfully reconstructs the detailed waveform from average value.

Step change of duty cycle. Figures 13, 14, and 15 show the response of output voltage and inductor current to a step change of the duty from 0.8421 to 0.7895. The output voltage is expected to decrease from 800 volts to 750 volts. The waveforms based on the SD, SSA and Hybrid models, are shown. In Fig.15, the SSA sub-model runs during the first three time divisions and the SD sub-model runs during the following five time divisions. The time scale is 200 micro seconds/division; The dynamic response is much larger than the switching ripple. However, the Hybrid model still successfully reconstructs the detailed waveform from average value.

Step change of source voltage. Figures 16, 17, and 18 show the response of output voltage and inductor current to a step change of the source voltage from 950 volts to 1000 volts. The waveforms based on the SD, SSA and Hybrid models, are shown. In Fig.18, the SSA sub-model runs during the first three time divisions and the SD sub-model runs during the following five time divisions. The time scale is 200 micro seconds/division; The dynamic response is much larger than the switching ripple. However, the Hybrid model still successfully reconstructs the detailed waveform from average value.

Results show that the detailed waveform reconstructed by the Hybrid model is very similar to the corresponding waveforms obtained from SD model. All the curves obtained from the three models predict the same results on average value and signal of switching frequency component in both steady state and perturbation transient.

Time cost

The reconstruction of the waveforms and the saving of time cost under this hierarchical approach are then proved by the performance of the SD, SSA and Hybrid models from the simulation program running in the environment of VTB

The SSA and SD models run in two different applications. The SSA model runs in VTB all the time. Since the SD model only runs for a small fraction of the hybrid time interval, the duty cycle in the SD time interval can be kept at a constant value. So the SD model runs under open loop control in the VXE Plug In [11] (a visualization tool in VTB). The SD model runs only 10% of the time with initial parameters (including the duty cycle) provided by the SSA model. Running the SD model open loop with constant duty cycle eliminates potential transients caused by mismatch in the initial conditions of the state variables provided by the SSA model. Fig. 19 shows the detailed waveform of the input current I_g that is observed in the 10%(in this case, two cycles) of each Hybrid model time interval in which the SD model runs. In the remaining 90% of the Hybrid model time interval, only the SSA model runs, so there is no SD model waveform to show. In VXE, the "chopped" waveform in Fig. 19 can be temporally compressed by throwing away the blank time intervals. In this way a continuous detailed waveform is reconstructed as shown in Fig. 20. Compare this waveform to the 100% detailed waveform in Fig. 21. We can see that in steady state they look alike except that the time scale in Fig.21 is 10% of that in Fig. 20.

From Table 1, we can see that the SSA time step will be the determining factor of the time cost. The time cost will be saved by increasing the SSA time step. The time costs of getting a 20% and a 100% waveform details are very close. The reason is that the SD model does not run in VTB, but in VXE Plug In. Although we have no idea of the time cost of running the SD model in VXE Plug In under current version, it is still reasonable to expect that less percentage of details will cost less CPU time and other resources.

Table 1: Time cost for running the SSA model in VTB

SSA time step	Hybrid time interval	Percentage of details	Simula-tion time	Time cost
100 μs	1 ms	20%	100 ms	32.077 s
100 μs	1 ms	100%	100 ms	34.610 s
200 μs	2 ms	10%	100 ms	23.103 s
200 μs	2 ms	50%	100 ms	22.763 s

4. Discussion

Comparison of the result by accuracy

Comparing the results shown in Appendix A, we can see that the detailed waveform of switching frequency component is well reconstructed by the Hybrid model both in steady state and perturbation transient.

It is noticed that when the simulation swaps between two models, there is a transient with resonance frequency of the LC filter. It is not clear why this happens. However, this transient is small, and it is damped out in a few cycles. A possible reason is that some native variables in the ACSL Integration algorithm are not reinitialized at the swapping point, or it may be caused by a small error between the average state variables of the SSA model and those of the SD model. It should be fixed with further study when the simulation program is written in a code like c++ in which the native integration variables can be easily

reinitialized. Further, this phenomenon does not invalidate the principles of the hierarchical approach. One way to solve this problem is to iterate the calculation until the transient diminishes before the time step goes forward[10].

Comparing these figures reveals that the waveform reconstruction algorithm adequately approximates the response.

Comparison of the result by time cost

Because of the high switching frequency, SD simulations are computationally intensive since the time step must be much smaller than the switching period. Thus the simulation time cost will rise with the switching frequency. These drawbacks have led to the simulation of these systems in the SSA model.

In the SSA model, the time step will not be limited by 1/ (2* frequency $_{switching}$), but by 1/ (2*frequency $_{natural}$). The frequency $_{natural}$ is the natural resonant frequency of inductor and capacitor. In Fig. 8, Fig.11, Fig.14 and Fig.17, we can see that the dynamic performance is well simulated with a potential of low time cost. However, the detailed waveform of switching frequency component is lost.

A tradeoff between low simulation time cost and sufficient resolution is reached by HYBID model which runs by swapping between the SSA and SD models. In Fig. 9, Fig.12, Fig.15 and Fig.18, the detailed switching behavior can be observed in the 10% of each Hybrid model time interval in which the SD model runs. What is more, the overall simulation time cost may potentially be lowered by running 90% of each Hybrid Model Time Interval in the SSA model with large time step. Also, the visualization Tool in VTB greatly enhances the performance of the hierarchical approach.

5. Conclusion

Simulation Performance indicate that the detailed switching behavior can be observed in the 10% of each Hybrid model time interval in which the SD model runs. Running 90% of each Hybrid Model Time Interval using the SSA model lowers the overall simulation time cost. This hierarchical or multilevel approach provides a possible way to simulate the detailed behavior of one component in a rather large switching circuit network. The hierarchical approach substantially increases the capabilities of the present models. Although the hierarchical method does not eliminate the need for detailed system simulation in all cases, it does provide a computationally economical alternative for a variety of studies useful in the design and evaluation of the electrical-mechanical systems that include switching power electronic circuits.

6. References

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11. Homepage of Virtual Test Bed: http://web.engr.sc.edu/vtb/.

7. Appendix

A. Simulation result:

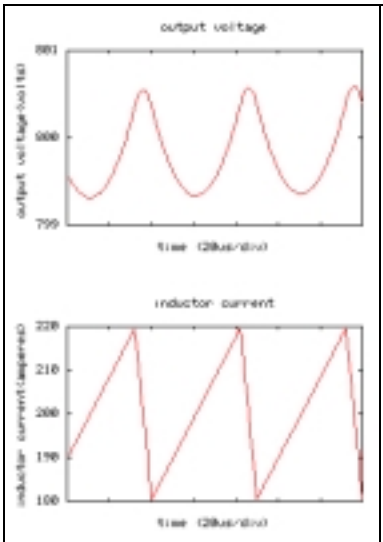

Fig.7 output voltage and inductor current at steady state of the SD model

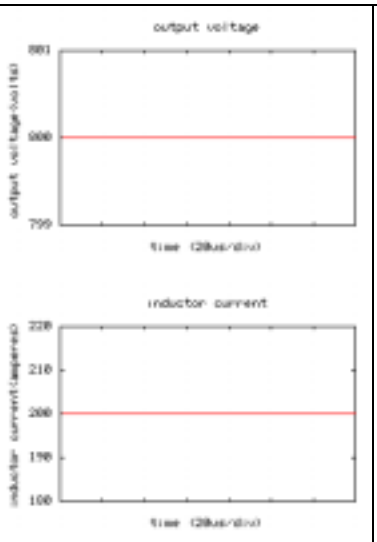

Fig.8 output voltage and inductor current at steady state of the SSA model

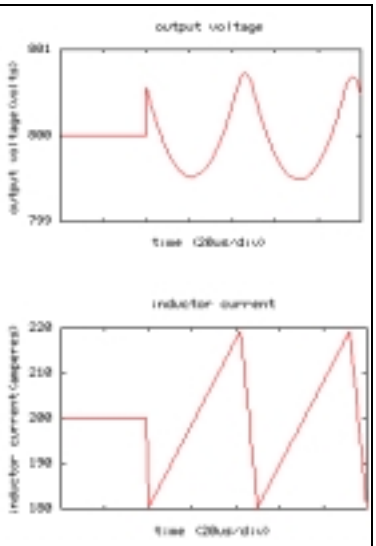

Fig. 9 output voltage and inductor current at steady state of the Hybrid model

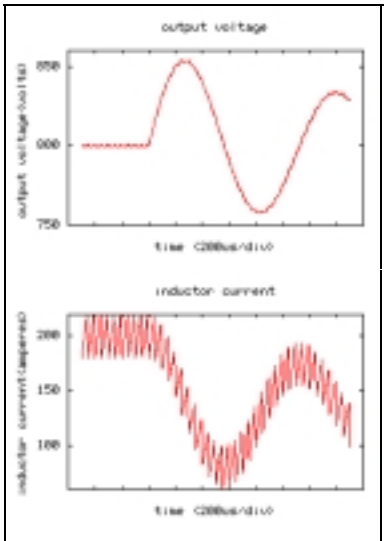

Fig.10 output voltage and inductor current of the SD model under a step decrease of resistive load from 4 ohms to 6 ohms.

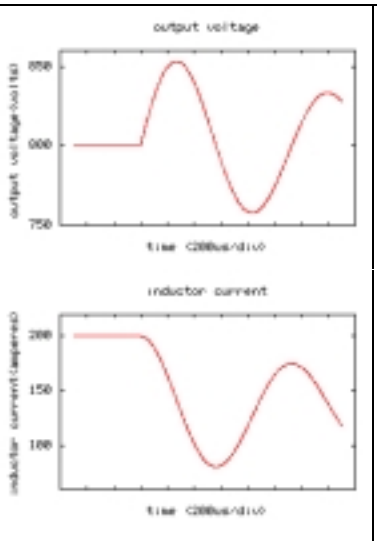

Fig.11 output voltage and inductor current of the SSA model under a step decrease of resistive load from 4 ohms to 6 ohms.

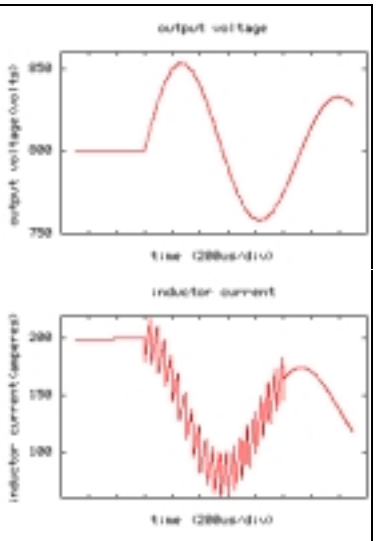

Fig.12 output voltage and inductor current of the Hybrid model under a step decrease of resistive load from 4 ohms to 6 ohms.

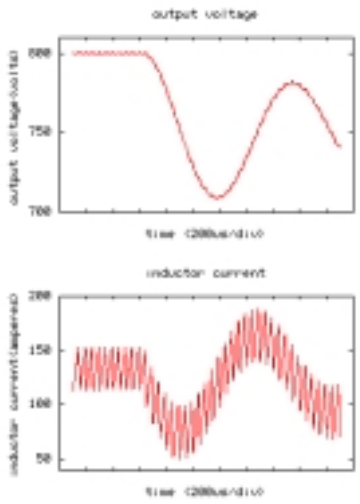

Fig.13 output voltage and inductor current of the SD model under a step decrease of duty cycle to change output voltage from 800 volts to 750 volts

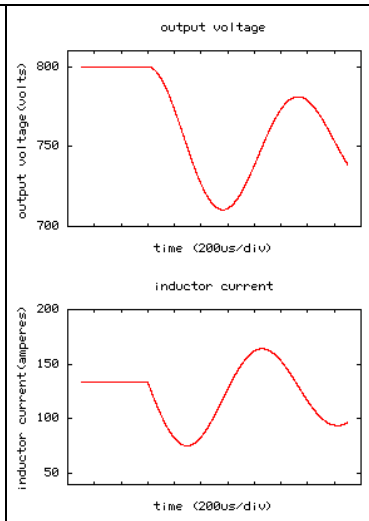

Fig.14 output voltage and inductor current of the SSA model under a step decrease of duty cycle to change output voltage from 800 volts to 750 volts

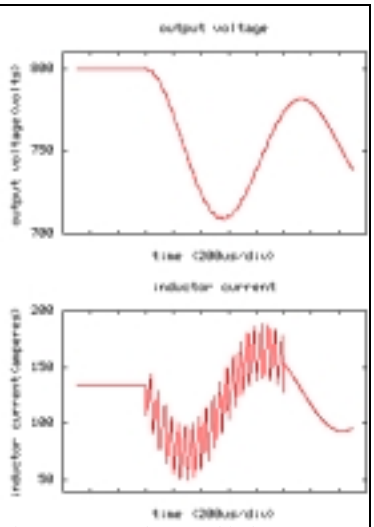

Fig.15 output voltage and inductor current of the Hybrid model under a step decrease of duty cycle to change output voltage from 800 volts to 750 volts

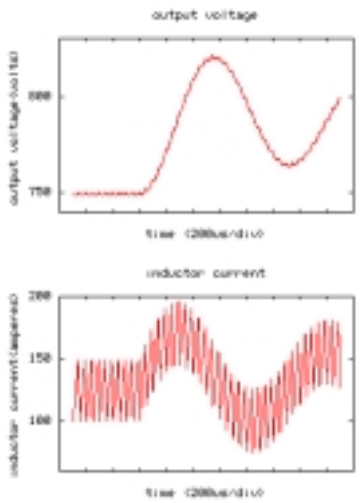

Fig.16 output voltage and inductor current of the SD model under a step increase of source voltage from 950 volts to 1000 volts

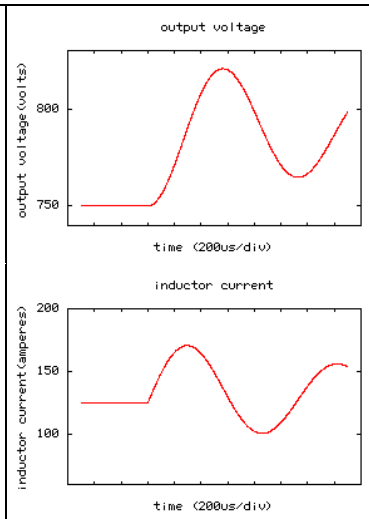

Fig.17 output voltage and inductor current of the SSA model under a step increase of source voltage from 950 volts to 1000 volts

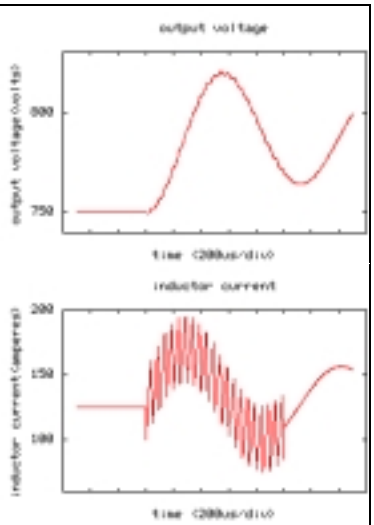

Fig.18 output voltage and inductor current of the Hybrid model under a step increase of source voltage from 950 volts to 1000 volts

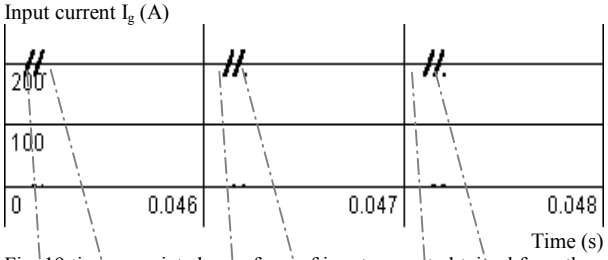

Fig. 19 time associated waveform of input current obtained from the SD model. In the intervals where no waveform is shown, only the SSA model runs.

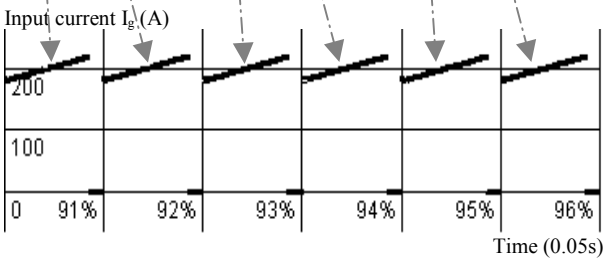

Fig. 20 time disassociated waveform of input current

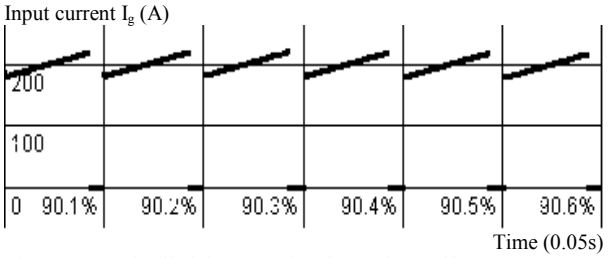

Fig. 21 100% detailed time associated waveform of input current

B. Derivation of average value of output voltage ripple:

In one half switching period, the output voltage ripple is

$$\Delta v_C(t) = \frac{1}{C}\int_0^t i_C ds$$

$$= \begin{cases} \frac{1}{C}\int_0^t \frac{\Delta i}{DT/2} s ds & , when 0 < t \le \frac{DT}{2} \\ \frac{1}{C}\int_{\frac{DT}{2}}^t \frac{\Delta i}{D'T/2}(\frac{T}{2} - s)ds + \frac{\Delta i DT}{4} & , when \frac{DT}{2} < t \le \frac{T}{2} \end{cases}$$

$$= \begin{cases} \frac{1}{C}\frac{\Delta i}{DT} t^2 & , when 0 < t \le \frac{DT}{2} \\ \frac{1}{C}\frac{\Delta i T}{4} - \frac{1}{C}\frac{\Delta i}{D'T}(\frac{T}{2} - t)^2 & , when \frac{DT}{2} < t \le \frac{T}{2} \end{cases}$$

So, the average value is

$$\overline{\Delta v_C} = \frac{2}{T}\int_{T/2} \Delta v_C dt$$

$$= \frac{2}{T}\int_0^{\frac{DT}{2}} \frac{1}{C}\frac{\Delta i}{DT} t^2 dt + \frac{2}{T}\int_{\frac{DT}{2}}^{\frac{T}{2}} [\frac{1}{C}\frac{\Delta i T}{4} - \frac{1}{C}\frac{\Delta i}{D'T}(\frac{T}{2} - t)^2]dt$$

$$= \frac{\Delta i_C T}{C}(\frac{D^2}{12} - \frac{D'^2}{12} + \frac{D'}{4}).$$

$$= \frac{\Delta i_C T}{C}(\frac{D^2}{12} + \frac{D'^2}{6} + \frac{DD'}{4}) \qquad (10)$$

8. Acknowledgements

The authors thank John Mookken for his help in building VTB native model of buck converter, and Michael Sechrest for his work on using Visualization Tools in VTB to display the waveform that is reconstructed in an animated scope-mode.