Testing of Digital Controllers Using Real-Time Hardware in the Loop Simulation

X. Wu, H. Figueroa, A. Monti
University of South Carolina
Columbia, SC29208, USA
Email: [wu6, figueroh, monti]@engr.sc.edu

***Abstract*— Designing and testing digital control systems for power electronics applications can be costly and time consuming. In this paper, a rapid, low-cost prototyping and testing procedure for digital controller design is proposed using Real-Time Hardware-In-the-Loop (RT HIL) Simulation. First, the control subsystem is prototyped using conventional simulation techniques. After the performance of the control logic is evaluated using non real-time simulation, the control subsystem is tested with RT HIL simulation. RT HIL simulation replaces the simulated control system with a real hardware controller, which interacts with other virtual models that are simulated in real-time. This increases the realism of the simulation and provides access to hardware features currently not available in software-only simulation models. Consequently, RT HIL makes the testing of new control equipment fast, safe and reliable. To perform RT HIL experiments, a real-time simulation platform has been implemented using Virtual Test Bed (VTB) and its real-time extension (RTVTB). As a demonstration of the proposed procedure, a digital controller for an H-bridge inverter is designed, implemented and tested. The frequency response analysis is also performed on the closed-loop system.**

I. INTRODUCTION

Designing and testing digital control systems for power electronics applications can be costly and time consuming. An effective approach for rapid prototyping and evaluation of power electronics systems and electric drives is RT HIL simulation. Currently, extensive research is being carried out in academia and industry in the development of simulation platforms suitable for RT HIL experiments [1][2][3]. However, many of the available commercial tools used to perform RT HIL simulation are expensive and use complex proprietary hardware. In order to be practical, the real-time simulation platform must be easy to set up for various tests.

In this paper, a rapid, low-cost design process for digital controllers for power electronics systems is proposed. VTB [4] and RTVTB [5][6] are utilized to implement an affordable real-time testing platform that allows the user to quickly specify the topology of the system under analysis. The design process and the software structure are described in detail. As a demonstration of the proposed procedure a digital controller for an H-bridge inverter is designed, implemented and tested. In the final experiment, the control software runs on the final target, while the plant model runs on the simulation platform. The RT HIL simulation results are compared with those of the fully simulated system. Finally, to determine how closely the RT HIL simulation match the behavior of the actual system, frequency response analysis is performed, and the results are analyzed.

II. SIMULATION ENVIRONMENT

The simulation environment is composed of the Virtual Test Bed (VTB) and its real-time extension (RTVTB).

VTB is a new environment for design, analysis, and virtual prototyping of multidisciplinary systems [7]. VTB is used at the prototyping stage to simulate the total system (plant and controller) and to evaluate its performance as a unit.

The real-time extension of VTB is called RTVTB [5]. To extend the possibility of the VTB to real-time applications, the Real-Time Application Interface (RTAI) [8] is utilized. This open-source software is used to create the hard real-time tasks that RTVTB needs to become a hard real-time Linux simulation environment. Being an adaptation of the Linux version of VTB, RTVTB shares the major parts of its architecture with the Windows version of VTB, which allows convenient importing of simulation models from the Windows platform to the RT Linux platform.

For VTB and RTVTB, the Signal Extension Resistive Companion solver (SRC) is currently implemented as the main core solver [4]. Its signal coupling feature allows natural coupling between hardware and software and enables RTVTB to perform HIL simulations.

III. DESIGN PROCESS OF DIGITAL CONTROLLERS WITH VTB AND RTVTB

The proposed process for rapid design and testing of digital control systems consists of three stages: system prototyping, RT HIL simulation and hardware testing.

A. Step One – System Prototyping

In this stage, the plant and the controller models are defined in VTB under Windows with full fidelity. The plant

model and the controller model are connected into one integral system in VTB, and the performance of the system is simulated.

B. Step Two – RT HIL Simulation

The RT HIL simulation provides an intermediate stage between simulation and deployment, where RTVTB models the plant, and the controller runs on the actual hardware. This approach can better replicate the real operational condition, and hence reduces the risk and cost of the final hardware testing.

C. Step Three – Hardware Testing

The final stage is the testing of the hardware controller over the actual target system.

The whole design process proposed above can be illustrated by Figure 1.

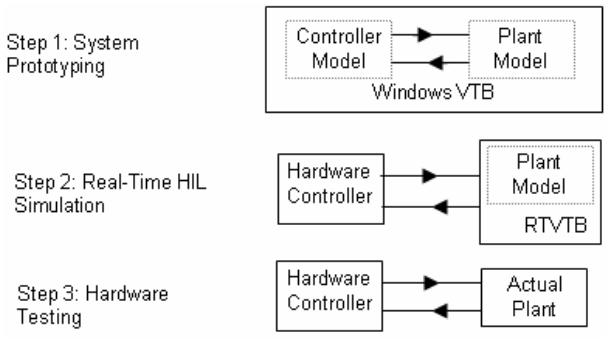


Fig. 1. Design Process of Digital Controllers with VTB and RTVTB

IV. APPLICATION EXAMPLE

A digital controller for an H-bridge inverter is designed using VTB, and then tested through HIL experiments. The system is illustrated in Figure 2. An averaged-value model is used to simulate the H-bridge inverter.

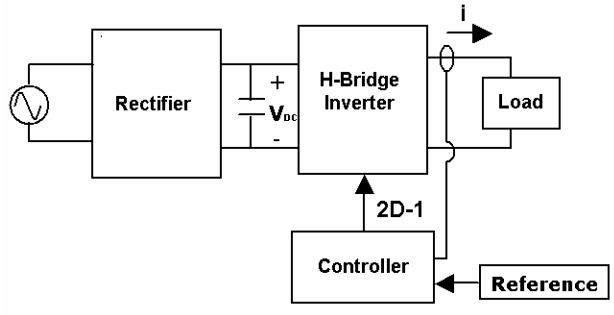


Fig. 2. The H-bridge inverter system

A. Design of the Controller

A proportional-integral (PI) controller is chosen for this application example. Figure 3 shows the block diagram of the complete system.

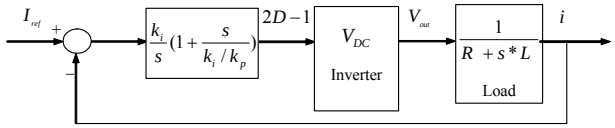


Fig. 3. Simplified block diagram of inverter-controller system

Equation 1 represents the averaged-value model of this H-bridge inverter.

$$V_{out}(s) = V_{DC} \times (2D - 1) \tag{1}$$

Where $V_{out}(s)$ is the output voltage of the inverter, D is the duty ratio of the switches of the inverter, V_{DC} is the DC bus voltage, R and L are the resistance and the inductance of the load respectively, I_{ref} is the current reference and i is the output current passing through the load. The parameters used in this experiment are listed as follows:

V_{DC} = 41V, R = 0.01Ω and L = 1mH

The open loop transfer function of the plant in the Laplace domain can be written as:

$$G_p(s) = \frac{I(s)}{X(s)} = \frac{V_{DC}}{R + L * s} \tag{2}$$

Where X = 2D-1

Choosing the bandwidth

$$\varpi_{BW} = 2\pi \times 100\,Hz = 628\,rad/s$$

and the phase margin

$$\varphi_{PM} = 50^\circ$$

To compensate for the delay effect caused by the D/A or A/D conversion and by the signal transition between the plant and the controller, the phase margin is modified as:

$$\varphi^*_{PM} = 50^\circ + \Delta\varphi = 50^\circ + \frac{\varpi_{BW} \times T_s}{2} = 54.5^\circ$$

Choosing the sampling rate of the controller $T_s = 250\mu s$ (the minimum time step that can be achieved in real-time simulation - its validity will be demonstrated in the following subsection), the parameters of the PI controller are:

$$k_p = 0.0123\,,\ k_i = 5.7163$$

The open loop transfer function of the plant in the Laplace domain can be written as:

$$G_o(s) = \frac{0.506s + 234.4}{0.001s^2 + 0.01s} \quad (3)$$

B. Stability Analysis

The mixed signal solver uses the Trapezoidal integration method. Therefore, the system representation can be discretized as:

$$G_o(Z) = \frac{0.506\frac{2}{T_c}\frac{Z-1}{Z+1} + 234.4}{0.001(\frac{2}{T_c}\frac{Z-1}{Z+1})^2 + 0.01\frac{2}{T_c}\frac{Z-1}{Z+1}} \quad (4)$$

The main stability issue of this system is related to the delay introduced by the signal processing, A/D and D/A conversion and model integration. With a proper sampling frequency, we can approximate the system as a hybrid system with an internal one-time-step delay. Based on this estimation, the system characteristic function can be derived as in Equation 5, and the root locus of the system with different sampling periods is shown in Figure 4.

$$1 + \frac{G_o(Z)}{Z} = 0 \quad (5)$$

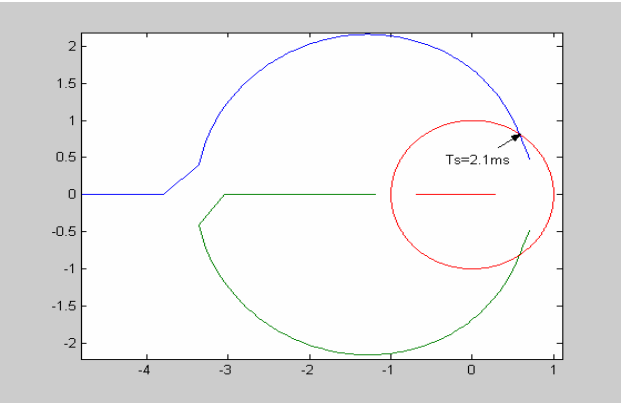


Fig. 4. Root locus of the discrete hybrid system

As can be seen from Figure 4, the system becomes unstable when the time step is bigger than 2.1ms. With the complexity of the system under test, the computing power, and the data transmission speed of the equipment available, the minimum time step that can be achieved while satisfying the real-time constraints is 250μs. Thus, in the experiment, this is the time step chosen.

V. Experimental Results

A. VTB Windows Simulation

The entire system is simulated using VTB under Windows to test the performance of the controller, as depicted in Figure 5.

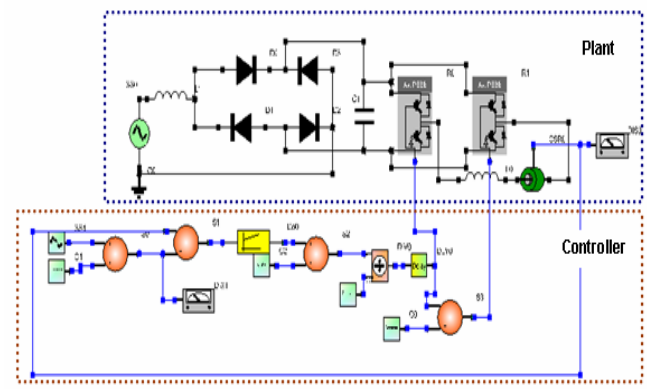


Fig. 5. Schematic of the entire system: the plant subsystem (H-bridge inverter) and the control subsystem (digital controller).

A sinusoidal waveform with amplitude of 2 V, frequency of 10Hz, and offset of 2.5 V is applied as the reference signal. The simulation results are shown in Figure 6.

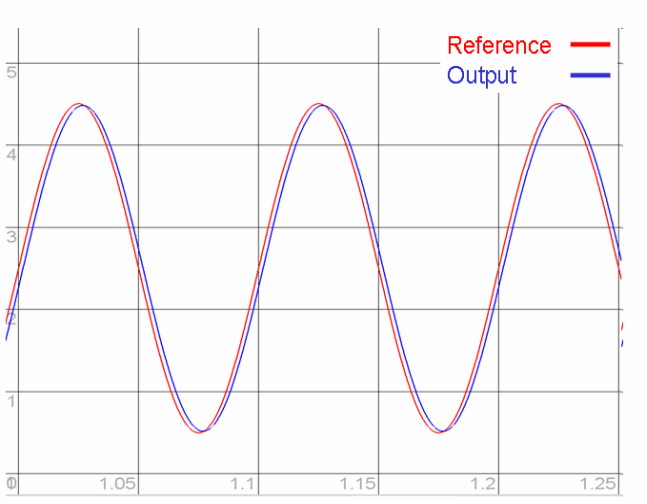


Fig. 6. Closed-loop VTB Windows simulation results

B. RT HIL Simulation

To perform RT HIL simulation, the plant and controller are separated into two subsystems. The controller subsystem is implemented in the microcontroller, while the plant subsystem is simulated in RTVTB. A real-time clock model and two external interface models are inserted into the plant subsystem, as shown in Figure 7.

This new stage of testing adds significant insights to the

final implementations such as:

- Real-time constraints.
- Quantization effects given by ADC and PWM units.

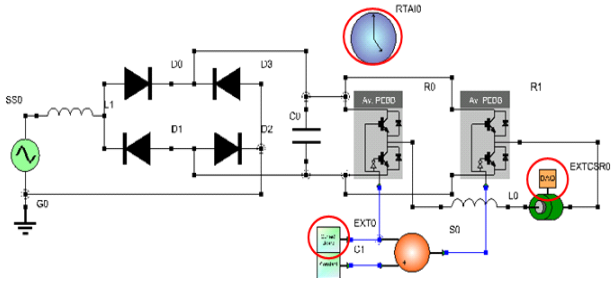


Fig. 7. Schematic of the plant subsystem

- Real-Time clock model

  The real-time clock model is used to synchronize RTVTB and a real-time kernel module implemented using RTAI. This module is a real-time task running at a very high priority.

- External interface model

  An interface model is implemented to interface VTB with the external ports of an Advantech PCI-1710 card. Employing Comedi Linux drivers [11], this model is able to access the digital and analog channels of this commercial DAQ card. The model is used for communication between the simulation process and the real world.

This system is exported into a Dell Precision™ Workstation 450n Linux machine for the execution of its RT HIL simulation. The simulation real-time clock is set to 250 microseconds. In this experiment, the external interface is used to output waveforms from the simulation environment to a scope and to allow interaction between RTVTB and the hardware controller.

In this application, the PI controller is implemented in a DS1104 dSPACE system [12]. The DS1104 controller board features several Analog and digital I/O and PWM units. At each time step, dSPACE takes the current feedback from RTVTB through data acquisition devices, and then compares it with the reference. The PI control algorithm is executed, and the control signal is sent to the plant model in RTVTB. Figure 8 depicts the structure of this configuration.

A signal generator provides the reference signal. This signal, as in the Windows simulation, is a 10 Hz sinusoidal waveform with amplitude of 2 V, and offset of 2.5 V. The offset maintains the signal within a range of 0V and 5V, which is the operating range for the analog digital converter of the Infineon microcontroller.

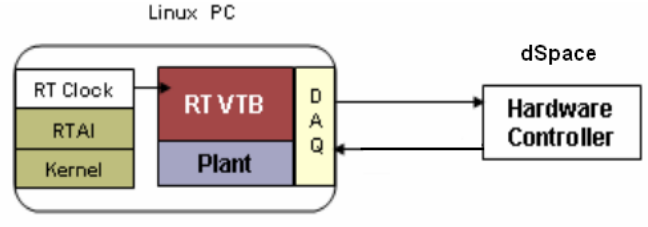


Fig. 8. Simulation Platform for RT HIL simulation

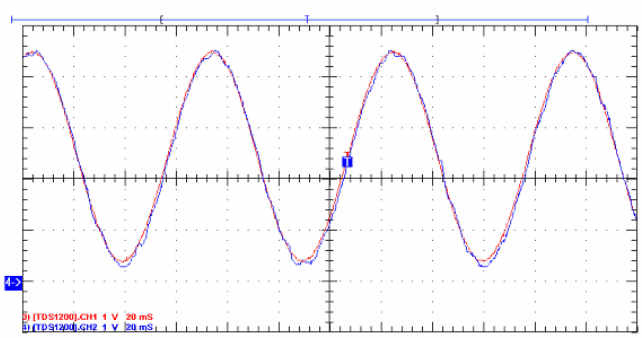


Fig. 9. HIL simulation results

The results of the experiment, depicted in Figure 9, are consistent with the previous Windows simulations shown in Figure 6. Therefore, these results confirm that the platform we have designed performs accurate RT HIL simulation, more quickly and at lower cost than currently available commercial tools.

C. *Frequency Response Analysis*

To determine how the RT HIL simulation matches the behavior of the actual system, frequency response analysis is performed for the following cases: approximated system transfer function in MATLAB®, VTB simulation, and finally RT HIL simulation.

The theoretical frequency response is calculated using MATLAB. A one-time-step delay (i.e. $T_d = T_s$) block is introduced between the controller and the plant subsystem to approximate the effects of the delay introduced by the communication between the hardware controller and the simulation platform, as explained in the Stability Analysis section. The block diagram of the resulting system is shown in Figure 10.

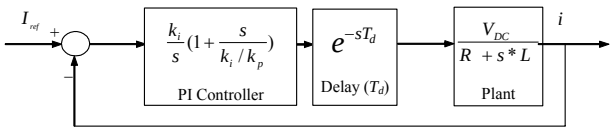


Fig.10 Block diagram of the system for the frequency analysis

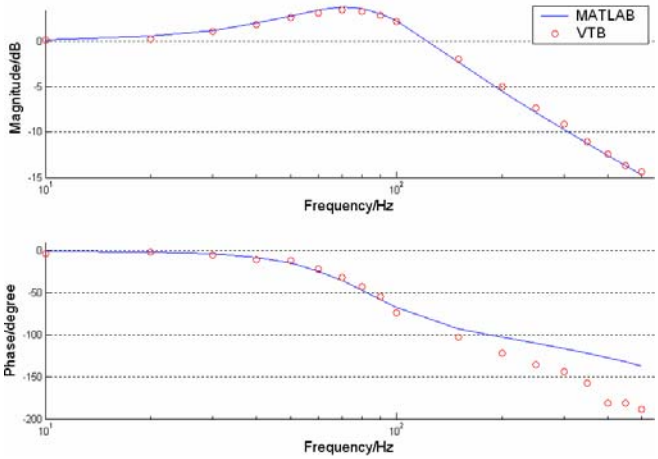
The delay is approximated using the Taylor series approximation of the exponential function. The final transfer function of the closed-loop system is:

$$G_{sys} = \frac{G_{os}(s)}{1+G_{os}(s)}$$

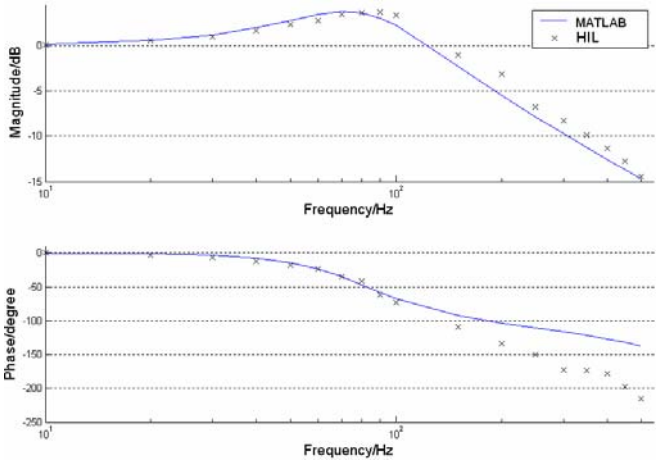
Where:

$$G_{os}(s) = (k_p + \frac{k_i}{s}) * \left(1 + (-s\,T_d) + \frac{(-s\,T_d)^2}{2} + \frac{(-s\,T_d)^3}{6}\right) * \frac{V_{DC}}{R + s * L}$$

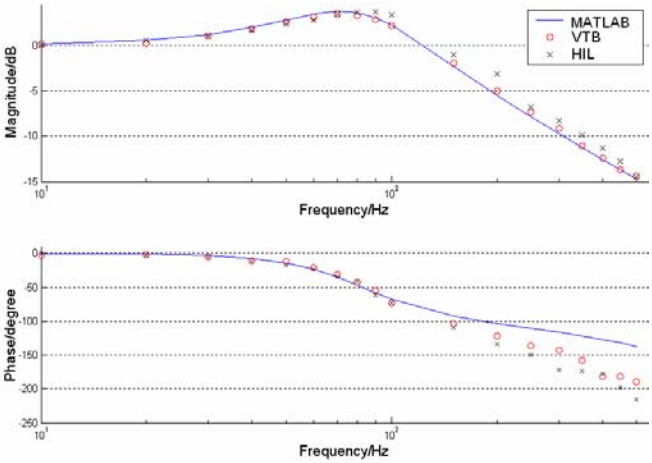
Then, the frequency response analyses are performed on VTB Windows simulation and RTVTB HIL simulation. In these cases, the frequency of the reference signal is changed from 10Hz to 100Hz in steps of 10Hz and from 100Hz to 500Hz in steps of 50Hz. The Bode plots of the experimental points are compared to the theoretical Bode plots from MATLAB, as shown in Figure 11.



(a) MATLAB and Windows VTB



(b) MATLAB and RTVTB HIL



(c) MATLAB, Windows VTB and RTVTB HIL

Fig. 11. Frequency analysis results

As it can be observed in Figure 11, the magnitude plot of the RT HIL simulation matches closely with that of the Windows VTB and MATLAB simulation. However, the phase plots of the RT HIL and VTB differ from the theoretical curve at frequencies higher than 100 Hz. The delay in the Windows VTB simulation and the RT HIL experiment is the principal cause of this difference.

In contrast to MATLAB, VTB considers temperature losses and internal resistance of the virtual models, such as the inverter, the diodes and the current sensors. The time response of the plant subsystem is governed by the ratio between the resistance and the inductance of the load (R/L). In VTB the equivalent resistance R_{eq} is equal to R plus the parasitic resistances; therefore, the delay increases in the Windows VTB and RTVTB.

Figure 12 shows the comparison between the phase plot of the HIL frequency response and a theoretical phase plot of the system using two-time-step delay ($T_d = 2T_s$). The HIL points fit this theoretical curve much better than the one using $T_d = T_s$.

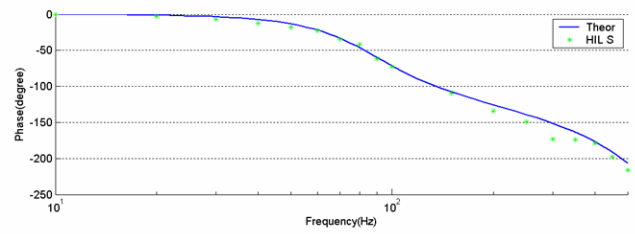


Fig. 12 Theoretical phase plot using two time-step delay

This plot indicates that the RT HIL simulation approach introduces an extra delay that is noticeable at higher frequencies. One time-step delay is a natural consequence of using digital controllers. This delay should be compensated in the design of the control system.

Additionally, an extra delay appears because the simulation platform and the digital controller are not synchronized.

VI. CONCLUSIONS

An affordable and reliable RT HIL simulation platform is implemented using VTB and RTVTB as simulation environments. Using this platform, real-time and the hardware-in-the-loop concepts are applied to develop a complete design process that supports the aspects of incremental virtual prototyping.

As an example, a digital controller for an H-bridge inverter is designed. Stability issues and time constraints are analyzed for the proper selection of the simulation time step. Results from the RT HIL experiment are consistent with those of the Windows VTB simulation.

The frequency response analysis shows a good match between the RT HIL experiment and the actual system. The effect of the extra time delay introduced by the HIL simulation is also discussed. The results show a coherent behavior and provide a better understanding of the potential and limitations of HIL testing.

In conclusion, this application demonstrates the effectiveness of the RT HIL simulation approach to the design and testing of digital controllers.

ACKNOWLEDGMENT

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