Two-Step Parameter Extraction Procedure With Formal Optimization for Physics-Based Circuit Simulator IGBT and p-i-n Diode Models

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***Abstract*—A practical and accurate parameter extraction method is presented for the Fourier-based-solution physics-based insulated gate bipolar transistor (IGBT) and power diode models. The goal is to obtain a model accurate enough to allow switching loss prediction under a variety of operating conditions. In the first step of the extraction procedure, only one simple clamped inductive load test is needed for the extraction of the six parameters required for the diode model and of the 12 and 15 parameters required for the nonpunch-through (NPT) and punch-through (PT) IGBT models, respectively. The second part of the extraction procedure is an automated formal optimization step that refines the parameter estimation. Validation with experimental results from various structures of IGBT demonstrates the accuracy of the proposed IGBT and diode models and the robustness of the parameter extraction method.**

***Index Terms*—Insulated gate bipolar transistor (IGBT) model, optimized parameter extraction, parameter extraction, power diode model, semiconductor modeling.**

I. Nomenclature

Parameters marked with an asterisk $(*)$ apply to both the diode and IGBT.

a	Impact ionization coefficient (cm^{-1}).
a	Diode reverse recovery current slope $(\mathrm{A}\cdot\mu\mathrm{s}^{-1})$.
a_i	Ratio of IGBT inter-cell to total die area.
A	Device area* (cm^2).
α	Impact ionization coefficient (cm^{-1}).
b	Impact ionization coefficient $(\mathrm{V}\cdot\mathrm{cm}^{-1})$.
b	Ratio of electron to hole mobility.
C_{CE}	IGBT collector–emitter capacitance (F).
C_{dep}	IGBT depletion layer capacitance (F).
C_{disp}	IGBT displacement capacitance (F).
C_{GC}	IGBT gate–collector (Miller) capacitance (F).
C_{GE}	IGBT gate–emitter capacitance (F).
C_{ies}	IGBT input capacitance (F).
C_{oes}	IGBT output capacitance (F).
C_{OX}	IGBT oxide capacitance $(\mathrm{F}\cdot\mathrm{cm}^{-2})$.
C_{res}	IGBT reverse transfer capacitance (F).
c_{xy}	Discrete cross correlation of signals x and y.
D	Ambipolar diffusivity* $(\mathrm{cm}^2\cdot\mathrm{s}^{-1})$.
D_{pH}	Hole diffusivity in the IGBT buffer layer $(\mathrm{cm}^2\cdot\mathrm{s}^{-1})$.
E	Electric field* $(\mathrm{V}\cdot\mathrm{cm}^{-1})$.
E_C	Critical electric field for breakdown $(\mathrm{V}\cdot\mathrm{cm}^{-1})$.
E_{SW}	Total switching energy (mJ).
ε	Permittivity of silicon* $(\mathrm{F}\cdot\mathrm{cm}^{-1})$.
f_e	Error figure for optimization.
h_n	N^+ emitter recombination coefficient* $(\mathrm{cm}^4\cdot\mathrm{s}^{-1})$.
h_p	P^+ emitter recombination coefficient* $(\mathrm{cm}^4\cdot\mathrm{s}^{-1})$.
I_A	Diode anode current (A).
I_C	IGBT collector current (A).
I_{CM}	IGBT peak collector current (A).
$I_C(0+)$	IGBT initial tail current height (A).
I_{disp}	IGBT displacement current (A).
I_F	Forward (on-state) current* (A).
I_k^τ	IGBT current tail normalization coefficient (A).
I_{mos}	IGBT MOSFET channel current (A).
I_{n1}	Electron current at anode end of carrier storage region (A).
I_{n2}	Electron current at cathode end of carrier storage region (A).
I_{p1}	Hole current at anode end of carrier storage region (A).
I_{p2}	Hole current at cathode end of carrier storage region (A).
I_{QH}	IGBT buffer layer charge control current (A).
I_{RM}	Peak diode reverse recovery current (A).
I_{sne}	IGBT buffer layer minority carrier saturation current (A).
J	Maximum current density* $(\mathrm{A}\cdot\mathrm{cm}^{-2})$.
k	Discrete cross correlation delay parameter (samples).
K_{pl}	IGBT MOSFET transconductance $(\mathrm{A}\cdot\mathrm{V}^{-2})$.
L_E	Kelvin emitter inductance (H).
l_m	IGBT intercell half-width $(\mu\mathrm{m})$.
L_{pH}	IGBT buffer layer hole diffusion length $(\mu\mathrm{m})$.
L_S	Circuit stray inductance (H).
λ	IGBT MOSFET channel shortening parameter (V^{-1}).
λ_{WE}	Proportion of cycle used for waveform evaluation.
M	Number of base points stored for Tabu list.
N	Window length for cross correlation (samples).

Manuscript received November 11, 2004; revised July 18, 2005. This work was supported by the U.S. Office of Naval Research under Grants N00014-00-1-0131, N00014-02-1-0623, and N00014-03-1-0434 and by the Schiff Foundation, Cambridge University. Recommended by Associate Editor Y. C. Liang.

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Digital Object Identifier 10.1109/TPEL.2005.869742

N_B	Drift region (base) doping concentration* (cm^{-3}).
N_H	Buffer layer doping concentration (cm^{-3}).
n_i	Intrinsic carrier concentration*(cm^{-3}).
p	Ambipolar carrier density* (cm^{-3}).
p_{H_0}	IGBT hole concentration at P^+ emitter/buffer layer junction (cm^{-3}).
p_{HW}	IGBT hole concentration at buffer layer/drift region junction (cm^{-3}).
p_{x1}	Ambipolar carrier density at anode end of carrier storage region* (cm^{-3}).
p_{x2}	Ambipolar carrier density at cathode end of carrier storage region* (cm^{-3}).
q	Unit electron charge*($= 1.6 \times 10^{-19}$ C).
Q_{RR}	Diode reverse recovery charge (C).
r_{xy}	Continuous cross correlation of signals x and y.
ρ	IGBT duty ratio in switching cycle.
T_0	Diode reverse recovery parameter (s).
T_1	Diode reverse recovery parameter (s).
T_A	Diode reverse recovery parameter (s).
t_{on}	IGBT on-state duration in switching cycle (s).
T_S	Period of switching cycle (s).
T_{WC}	Length of window used for cross correlation (synchronization) (s).
τ	Continuous cross correlation delay parameter (s).
τ_{BF}	IGBT buffer layer lifetime (s).
τ_{eff}	PT IGBT effective lifetime (s).
τ_{HL}	High-level lifetime*(s).
τ_0	Initial estimate of diode lifetime (s).
τ_{pH}	IGBT hole lifetime in buffer layer (s).
τ_{RR}	Diode reverse recovery time (s).
V_{BD}	Diode breakdown voltage (V).
V_{BR}	IGBT breakdown voltage (V).
V_{CE}	IGBT collector–emitter voltage (V).
V_{CM}	IGBT peak collector–emitter voltage during turn-off (V).
V_{d_1}	Anode depletion layer voltage* (V).
V_{d_2}	Cathode depletion layer voltage * (V).
V_{DC}	Supply voltage (V).
V_{DS}	IGBT MOSFET drain–source voltage (V).
V_{GG}	IGBT gate drive voltage (V).
V_{GS}	IGBT MOSFET gate–source voltage (V).
V_{PT}	NPT IGBT punch-through (PT) voltage (V).
V_{RRM}	Diode peak reverse recovery voltage (V).
V_{TH}	IGBT MOSFET threshold voltage (V).
W_B	Drift region (base) width* (μm).
W_H	IGBT buffer layer width (μm).
x_1	Boundary position of anode end of carrier storage region* (μm).
x_2	Boundary position of cathode end of carrier storage region* (μm).

II. Introduction

In RECENT years, the characteristics of insulated gate bipolar transistors (IGBTs) have been greatly improved. For example, with the application of advanced lifetime killing technology and structure development [1], the fourth generation IGBTs [trench-gate punch-through (PT)], which have been available in the market for some time, exhibit fast turn-off speed and low saturation voltage. Buffer-layer IGBTs also exhibit tail-free turn-off current under high voltage conditions [2]. The application of light PT [3] and field-stop technology now offers the new fifth generation IGBT with superior characteristics. These external characteristics, brought about by internal device design changes, can only be accurately modeled by a physics-based (analytical) IGBT model. However, in spite of the accuracy of physics-based IGBT models, either overly complex or inaccurate parameterization procedures often discourage electronic engineers from attempting to use IGBT models in their system designs.

Reviewing the IGBT circuit model parameter extraction methods described in the literature shows that further work must be done in the field. The parameter extraction provided for the accurate and comprehensive Hefner model [2], [4] is so complex that it is not practical for electrical engineers. The extraction method proposed in [5] is only for the lumped-charge IGBT model. In [6], the parameter extraction for the Hefner model was further developed with seven very precise but complex experiments. The parameters extracted in [7] are used for IGBT behavioral models. In [8], the parameter extraction lacks detail.

One of the primary reasons for device and circuit simulation in power electronic system design is estimation of power losses. The significant source of such losses is generally the switching devices. Hence, an accurate and physically based model is required, as the simulations must be valid over a wide range of conditions. This is also the case in determining other characteristics such as electromagnetic compatibility.

Crucially, the parameters must be found for a good fit with the devices and circuit. In most power electronics circuits the IGBTs operate under clamped inductive switching with a free-wheeling diode. In order to obtain good switching loss estimates, an accurate physics-based model for the power diode is also needed.

In conclusion, accurate physics based models for the IGBT and diode are needed. On the other hand, the parameter extraction procedure has to be simple enough to be practical. In order to meet these conflicting requirements in this work we propose a two-step parameter extraction, consisting of a simple parameter estimation based on datasheet data and a single clamped inductive measurement, followed by an automated optimization procedure to refine the extracted parameters.

Previous attempts at an automated parameterization procedure have concentrated on either fitting dc characteristics [9] or key performance indicators, for example reverse recovery currents and times in the case of the power diode [10], [11]. None allow a model to be fitted sufficiently to produce accurate switching power loss estimates.

This paper describes parameter extraction and refinement using a formal optimization procedure. One of the goals is to provide a complete extraction procedure for IGBT and power diode that describes in sufficient detail both the initial parameter estimation and the optimization procedure. The extraction procedure is valid for different families of IGBTs such as PT, nonpunch-through (NPT), field-stop, and trench gate. The physics-based model has been proven accurate for all of these devices [12]–[14]. The procedure is based on accurate device and circuit models coupled with an optimization algorithm and hardware data acquisition. All of these run from or within MATLAB. However, once the parameter extraction is complete,

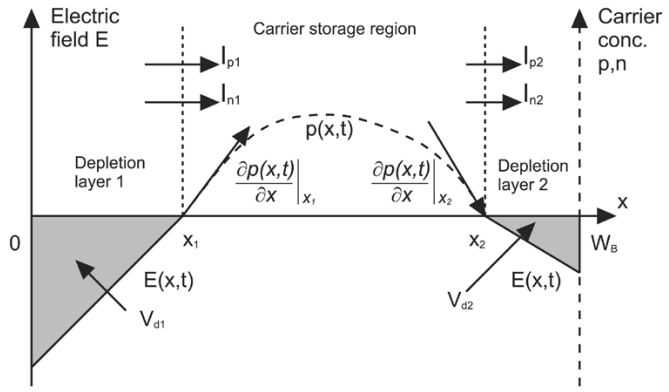

Fig. 1. General arrangement of carrier storage region and depletion layers in the FBS model, shown for the diode and the n-base region of the IGBT; the doping is NB. The anode (IGBT collector terminal) is on the left, and the cathode (IGBT emitter terminal) is on the right. The carrier density $p(x,t)$ is solved for the boundary carrier density gradients $\partial p/\partial x|_{x1}$, $\partial p/\partial x|_{x2}$, and boundary positions x_1 and x_2.

the parameters may be used for the models implemented on any platform, including circuit simulators such as PSpice.

III. Physics-Based Circuit Simulator IGBT and Diode Models

Being a conductivity-modulated power device, the behavior of an IGBT or a p-i-n diode depends heavily on the carrier distribution in its wide drift region. For diodes, the carrier distribution across the wide drift region is approximately one-dimensional (1-D). For IGBTs, it is 1-D across 90% of the drift region [12], and so may be reasonably assumed as such for the whole region provided some modifications are made.

Under these conditions, assuming high-level injection, the Ambipolar carrier diffusion equation (ADE) (1) describes the carrier dynamics

$$D\frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{\tau_{\mathrm{HL}}} + \frac{\partial p(x,t)}{\partial t} \tag{1}$$

where D is the ambipolar diffusion coefficient, τ_{HL} is the high-level carrier lifetime within the drift region, and $p(x,t)$ is the excess carrier concentration.

Most physics-based circuit simulator modeling approaches focus on the simulation of the drift region, and consequently implement the modeling of the ADE. The Fourier-based-solution (FBS) model is adopted in this research [12], [15]. For a more comprehensive description of the IGBT and diode models used in this work, refer to [12] and [16]. This approach preserves the essentials of the distributed nature of charge dynamics within the drift region and offers reasonable simulation speed while preserving satisfactory accuracy. It effectively reduces the PDE into a set of coupled first-order ODEs which may be solved in circuit simulators (e.g., PSpice [12], Saber) or general-purpose simulators (e.g., MATLAB/Simulink [17]). The representation used for the whole region is shown in Fig. 1, and the ADE requires boundary conditions of the carrier density gradients $\partial p/\partial x|_{x1}, \partial p/\partial x|_{x2}$ (dependent on the device current), and boundary positions x_1 and x_2. The carrier density $p(x)$ is solved using the FBS model, and the carrier densities p_{x1} and p_{x2} at the boundaries are used to generate the boundary conditions and device terminal voltage. The formulation of the boundary conditions depends on the device modeled, giving the device its characteristic behavior. Table I gives the relationships between the boundary carrier densities and currents for the diode and IGBT.

For p-i-n diodes, the P^+ and N^+ layers act as emitter regions when the diode is on. The electron and hole boundary currents I_{n1}, I_{p2} are given in terms of the boundary carrier densities p_{x1}, p_{x2} by the classic recombination equation [18]. For the IGBT, the MOS channel current I_{mos} can be found as a function of the gate–source voltage using the well-known MOSFET equation. At the left (anode) side of the drift region, different equations are used for the NPT and PT IGBT due to the structural differences. For the NPT IGBT, the emitter recombination equation is used to calculate the electron current element at the junction between the P^+ emitter and the N^- drift region. For the PT IGBT, the buffer layer formulation in [16] is used to obtain the hole current component I_{p1} at the junction between the N buffer layer and the N^- drift region. Some modifications required to take into account capacitive currents are described in detail in [12] and [16].

IV. Two-Step Parameter Extraction Procedure

The proposed parameter extraction procedure consists of two separate steps.

1) Initial Parameter Extraction—This is based on device datasheets and at most one clamped inductive switching experiment;
2) Optimization Procedure—Refinement of parameters through a formal optimization procedure.

Generally, there are three kinds of parameter extraction methodologies, which include: 1) simple estimation based on the empirical value range, 2) extrapolation according to the manufacturer's datasheet, and 3) extraction with simple experiments. To make the extraction procedure practical, the three methods are employed jointly.

Some of the diode and IGBT parameters listed in Tables II and III can be obtained from the datasheet or calculated based on textbook equations, so there is no need to use measurement for their extraction. Extra measurement can be used to verify the mathematical results. But some parameters, like IGBT carrier lifetime, have to be determined by experiment, which also needs to be simple. Accordingly, the clamped inductive load test experiment is used. The second step in the procedure is a formal optimization which may be completely automated. An advantage of this procedure is that inaccuracies in the initial parameter estimation may be corrected by the optimization procedure.

The parameter extraction process can be summarized in the following list and in Fig. 2:

a) initial estimates of parameters made from device datasheets and basic measurements;
b) measurement of device switching behavior, i.e., acquisition of switching waveforms;
c) simulation of circuit behavior using parameters estimated;
d) comparison of simulated and measured waveforms to produce an error value;
e) variation of the parameter values to minimize the error value.

TABLE I
BOUNDARY CURRENT FORMULATION FOR THE DIODE AND IGBT

	I_{n1}	I_{p1}	I_{n2}	I_{p2}
Diode	$qAh_p{p_{x1}}^2$	I_A-I_{n1}	I_A-I_{p2}	$qAh_n{p_{x2}}^2$
NPT IGBT	$qAh_p{p_{x1}}^2$	I_C-I_{n1}	I_{mos} (channel current)	I_C-I_{n2}
PT IGBT	I_C-I_{p1}	$I_{p1}=\frac{qAD_{pH}}{L_{pH}\sinh\left(\frac{W_H}{L_{pH}}\right)}\left[p_{H0}-p_{HW}\cosh\left(\frac{W_H}{L_{pH}}\right)\right]+I_{QH}$	I_{mos} (channel current)	I_C-I_{n2}

TABLE II
DIODE MODEL PARAMETER LIST

Symbol	Description	Step
A (cm^2)	Active die area	1
τ_{HL} (μs)	High-level lifetime	2
W_B (μm)	Drift region width	3
N_B (cm^{-3})	Drift region doping	4
$h_n h_p$ ($cm^4 s^{-1}$)	Emitter recombination parameters	5

TABLE III
IGBT MODEL PARAMETER LIST

Part	Symbol	Description	Step
MOS Gate	V_{TH} (V)	MOS threshold voltage	1
	K_{pl} (AV^{-2})	MOS transconductance coefficient	1
	λ (V^{-1})	Short-channel parameter	1
	C_{GE} (nF)	Gate-emitter capacitance	2
	C_{OX} ($nFcm^{-2}$)	Oxide capacitance	2
	l_m (μm)	Inter-cell half-width	2
Geometry	A (cm^2)	Effective die area	2
	a_i	Ratio of inter-cell to total die area	2
Collector Body	N_B (cm^{-3})	Doping concentration of N-drift region	3
	W_B (cm)	Width of N-drift region	3
	τ_{HL} (μs)	Carrier high-level lifetime in N-drift region	4
	τ_{BF} (μs)	Carrier lifetime in N buffer-layer (PT)	4
	h_p ($cm^4 s^{-1}$)	Hole recombination coefficient in emitter (NPT)	5
	W_H (cm)	Width of N-buffer layer (PT)	5
	N_H (cm^{-3})	Doping concentration of N-buffer Layer (PT)	5
	I_{sne} (A)	Minority carrier saturation current (PT)	5

Step e) is the optimization procedure. Once the error value has been determined, the parameters are varied and the simulation in step c) re-executed to produce a waveform valid for that set of parameters. This is again compared to the measured waveform in step 4), and the optimization continues accordingly. Once the parameters have converged to give a minimum error, the optimization procedure stops.

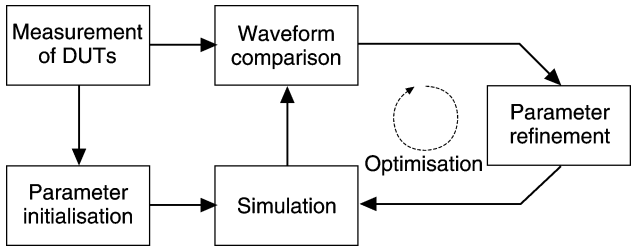

Fig. 2. Diagram showing the procedure of parameter extraction.

V. STEP 1: INITIAL PARAMETER ESTIMATION

A. Initial Parameter Estimation for Power Diodes

One of the major advantages of the physically-based diode model is that only six parameters from manufacturers are needed and can be easily estimated from the datasheets or from a single diode turn-off measurement.

Five important ratings given in the diode manufacturer datasheets are: i) repetitive maximum voltage $V_{RRM.}$, ii) dc forward current I_F, iii) reverse recovery charge $Q_{RR.}$, iv) reverse recovery peak current I_{RM}, and v) reverse recovery time. The following steps describe the parameter estimation.

1) Diode Area A: Since the maximum current density J is for most power diodes from 100 A · cm^{-2} to 150 A · cm^{-2}, the active die area A can be roughly estimated from the average forward dc current in the datasheet using

$$A = \frac{I_F}{J}. \tag{2}$$

A more precise estimate can be obtained by opening the device and measuring the actual die area.

2) Diode Lifetime τ_{HL}: Neglecting the recombination effect in the reverse charge, (3) is used to make an initial estimate τ_0 for the high-level lifetime

$$\tau_{\mathrm{HL}} \approx \tau_0 = \frac{Q_{\mathrm{RR}}}{I_F}. \tag{3}$$

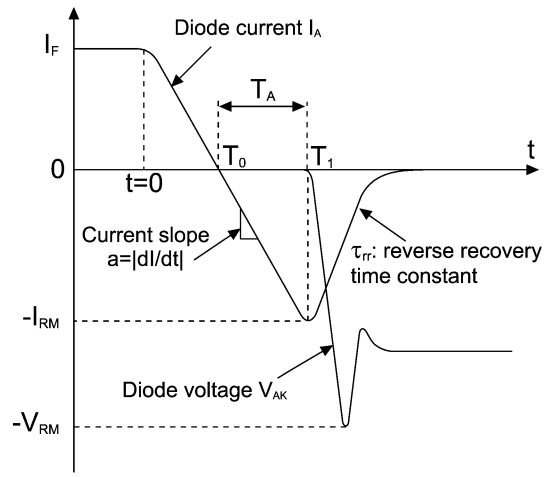

Fig. 3. Diode reverse recovery.

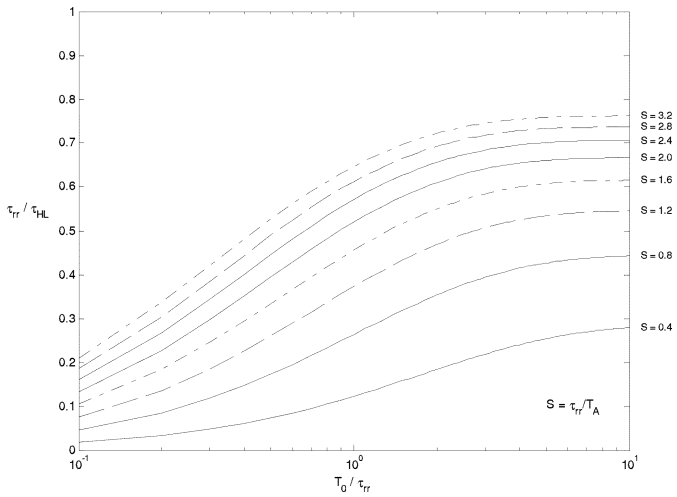

Fig. 4. Diode reverse recovery lifetime extraction.

In the case that the reverse recovery charge $Q_{\rm RR}$ in the datasheet is given for a temperature other than room temperature, the parameter τ_0 can be scaled accordingly [12]. A more accurate estimate for the lifetime may be made using an inductive turn-off measurement [19], [20]. This will only be necessary if the automated parameter optimization in Section V is not carried out.

The extraction of the lifetime using the inductive measurement refers to Fig. 3. After time T_1 the current waveform has the form

$$i(t) = -I_{RM} \exp\left(-\frac{t-T_1}{\tau_{\rm RR}}\right), \quad \text{for } t \geq T_1 \tag{4}$$

where $\tau_{\rm RR}$ is the reverse recovery time constant and can be extracted from the experimental reverse recovery current waveform. In [19], it is shown that the following relationship holds:

$$I_{RM} = a(\tau_{\rm HL} - \tau_{\rm RR})\left[1 - \exp\left(-\frac{T_1}{\tau_{\rm HL}}\right)\right]. \tag{5}$$

All parameters can be determined from the experimental waveform: current fall slope a, peak reverse current I_{RM}, and time T_1 at which it occurs, reverse recovery time constant $\tau_{\rm RR}$. The lifetime $\tau_{\rm HL}$ can be obtained by solving the implicit (5). Alternatively, following the approach of [20] the lifetime can be read from a graph. Substituting $I_{RM} = aT_A$ and $T_1 = T_0 + T_A$ (5) can be rewritten as

$$\frac{T_A}{\tau_{\rm RR}} = \left[\frac{\tau_{\rm HL}}{\tau_{\rm RR}} - 1\right]\left\{1 - \exp\left[-\frac{\tau_{\rm RR}}{\tau_{\rm HL}}\left(\frac{T_0}{\tau_{\rm RR}} + \frac{T_A}{\tau_{\rm RR}}\right)\right]\right\}. \tag{6}$$

In this expression there are three dimensionless quantities: $T_0/\tau_{\rm RR}$, $\tau_{\rm RR}/T_A$, and $\tau_{\rm RR}/\tau_{\rm HL}$. The first two are known and the third can be read from the graph in Fig. 4. Notice that parameter $S = \tau_{\rm RR}/T_A$ gives an indication of the snappiness of a diode and is related to the classical snappiness factor (also called softness factor).

3) Diode Drift Region Width W_B: The electric field (E) dependence of the ionization coefficients for electrons and holes in Si, α, has been shown to fit experimental data fairly well in the form as given in (7), [21]–[23]

$$\alpha_{n,p} = a \exp\left(\frac{-b}{E}\right) \tag{7}$$

where a varies between 7×10^5 and 3.8×10^6 $\rm cm^{-1}$ with a corresponding variation in b from 1.47×10^6 to 1.75×10^6 $\rm Vcm^{-1}$. Assuming breakdown in the bulk, an abrupt junction, equal ionization coefficients for holes and electrons, and a p^+-n^--n^+ structure, an expression for the breakdown voltage in terms of the parameters a, b, and the N-drift region (base) width, W_B, can be obtained

$$V_{\rm BD} = \frac{bW_B}{\ln(aW_B)}. \tag{8}$$

The N-drift region width, W_B, used in the model is derived based on (8) using $a = 1.07\times10^6$ $\rm cm^{-1}$, $b = 1.65\times10^6$ $\rm V\cdot cm^{-1}$, and the value of the breakdown voltage from the manufacturer's data sheet plus some margin.

4) Diode Drift Region Doping N_B: For purposes of the modeling and based on the empirical effective impurity doping concentration range ($6\times10^{13} - 2\times10^{14}$ $\rm cm^{-3}$) in the N-drift region, the doping concentration is assumed to be 10^{14} $\rm cm^{-3}$.

5) Diode Recombination Parameters h_n, h_p: The recombination parameters h_n and h_p control the amount of charge present in the diode during the on-state; their increase results in a reduction in stored charge and therefore a reduction in reverse recovery charge. An initial estimate of 1×10^{-14} $\rm cm^4\cdot s^{-1}$ may be made for both.

Fig. 3 shows typical reverse recovery current and voltage waveforms obtained from an inductive turn-off measurement. In the model, the lifetime is the dominant parameter affecting the recovery waveforms. With the correct high-level lifetime $\tau_{\rm HL}$, not only good matching of the reverse current can be obtained, but also a good match of the diode voltage waveform during turn-off, including overshoot and ringing, can be made. The first estimate of high-level lifetime, $\tau_{\rm HL}$, is given by the initial recovery time τ_0. A better estimate can be obtained by trying to match the reverse recovery current. After this, the N-base width estimate can be improved by trying to improve the matching of

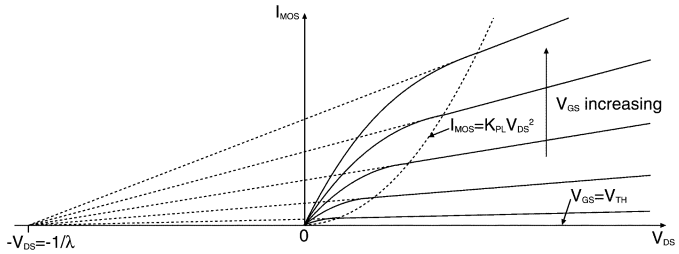

Fig. 5. Forward I–V characteristics of the IGBT MOS gate.

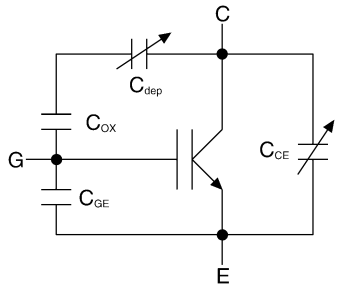

Fig. 6. IGBT capacitances.

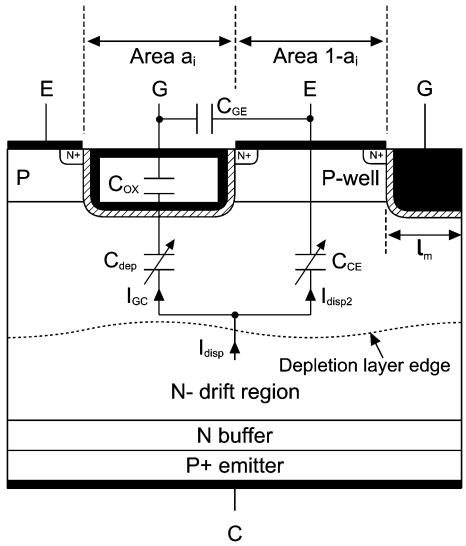

Fig. 7. Capacitance distribution diagram for a trench gate IGBT.

the diode voltage waveform. It has been found empirically that, compared with lifetime $\tau_{\rm HL}$, the width and doping of the N-drift region do not have significant effects on the reverse recovery current, but have an obvious effect on the diode voltage waveform in the simulation. The recombination parameters h_n and h_p affect the reverse recovery current—in particular the peak reverse recovery current I_{RM}—and should be used to improve the matching further.

B. Initial Parameter Estimation for IGBTs

The FBS IGBT model requires 12 and 15 nonsilicon parameters for the NPT and PT structure IGBTs, respectively. Table III lists the parameters, which are classified into three categories based on the related device part: MOS-gate, geometry, and collector body parameters.

Because a behavioral MOSFET model is used for the IGBT MOS gate, the relevant parameters can be extracted following the extraction procedure for a MOSFET. The information given in the manufacturers' datasheets is enough to extract these five parameters.

1) MOS Parameters: The first three MOSFET parameters, MOS threshold voltage $V_{\rm TH}$, transconductance coefficient K_{pl}, and short channel parameter λ, can be obtained from the known I–V characteristic curve, shown in Fig. 5. Note that this curve is only used for obtaining initial parameter estimates and is not used in further processing. The electron current $I_{\rm mos}$ that flows through the elemental MOSFET is a fraction of the total IGBT current I_C and can be calculated as

$$I_{\rm mos} = \frac{b}{b+1} I_C \tag{9}$$

where b is the ratio of electron and hole mobilities. The assumption of this fraction is necessary to obtain an initial estimate of the MOS parameters. The MOS channel voltage $V_{\rm DS}$ is approximately equal to the collector–emitter voltage $V_{\rm CE}$ during saturated operation of the channel $(V_{\rm DS} \geq V_{\rm GS} - V_{\rm TH})$.

2) IGBT Geometry and Capacitances: The active die area A can be measured directly by opening the device package. Another method is based on the empirical range of IGBT maximum current density J. Therefore, the active die area can be roughly estimated as

$$A = \frac{I_{\rm CM}}{J} \tag{10}$$

where $I_{\rm CM}$ is the peak collector current from the RBSOA curve given in the datasheet. Practically, the $I_{\rm CM}$ value is decided by many factors, not only the chip but also the package and heat extraction. Nevertheless, the range of current density J generally is 100 A $\cdot$ cm^{-2}–250 A $\cdot$ cm^{-2}.

The ratio of intercell area to total die area a_i can be extracted based on the capacitances in the datasheet. Figs. 6 and 7 show the IGBT capacitance distribution. It can be seen that the displacement current $I_{\rm disp}$, due to variation of the depletion region width, flows through two branches: the first branch is under the emitter terminal, which is represented by the collector–emitter capacitance $C_{\rm CE}$, while the other is the Miller capacitance branch, which includes collector-gate capacitance, $C_{\rm GC}$ and gate–emitter capacitance $C_{\rm GE}$. When the gate is shorted to the emitter ($V_{\rm GE} = 0$ V), the second branch only includes $C_{\rm GC}$. Using analysis in [24] and [15], the intercell ratio can be obtained as

$$a_i \approx \frac{\min\left(C_{\rm res}\right)}{\min\left(C_{\rm oes}\right)}. \tag{11}$$

Equation (11) is only valid under the condition that the collector–emitter voltage $V_{\rm CE}$ is sufficiently high to allow for an approximately uniform space-charge layer capacitance over the whole crystal area. Therefore, the minimum values of $C_{\rm oes}$ and $C_{\rm res}$ in the datasheet should be chosen, as a sufficiently high $V_{\rm CE}$ is reached at that point.

As shown in Figs. 6 and 7, the MOS oxide capacitance $C_{\rm OX}$, together with the series-connected depletion capacitance $C_{\rm dep}$ determines the gate–collector capacitance $C_{\rm GC}$, which is also called the reverse transfer capacitance $C_{\rm res}$ in datasheets and is commonly referred to as the Miller capacitance between gate

and collector. $C_{\rm OX}$ is the maximum value of the Miller capacitance when the depletion region under the gate area has not formed ($C_{\rm dep} = \infty$). That point corresponds to the maximum point of the $C_{\rm res}$ curve in the datasheet. $C_{\rm OX}$ is strictly the oxide capacitance per unit area, and therefore is written as

$$C_{\rm OX} = \frac{\max(C_{\rm res})}{Aa_i}. \tag{12}$$

The intercell half-width l_m is typically 5–15 μm. Along with the Miller capacitance $C_{\rm GC}$ it controls the length of the gate voltage plateau during switching; larger values of l_m give longer plateau durations.

The gate–emitter capacitance $C_{\rm GE}$ can be directly obtained from the input capacitance $C_{\rm ies}$ (measured gate–emitter capacitance when collector is shorted to emitter) provided in the datasheet. Since the input capacitance $C_{\rm ies}$ is the sum of the $C_{\rm GE}$ and the Miller capacitance $C_{\rm GC}$, and the former is much larger than the latter at higher voltages, $C_{\rm GE}$ can be chosen equal to $C_{\rm ies}$ at 100 V.

3) IGBT Drift Region Parameters: There are several different ways to extract the doping concentration of the drift region N_B. The first is the direct estimation based on the normal range of the drift region background doping, which is from 6×10^{13} to 2×10^{14} cm^{-3} for the IGBT device. The typical value, 1×10^{14} cm^{-3}, is generally chosen as the doping concentration N_B during the simulation. The second way is based on the relation between the doping concentration and the breakdown voltage [25] using

$$N_B = 2.88\times10^{17}V_{\rm BR}^{-1} \tag{13}$$

where $V_{\rm BR}$ is the breakdown voltage value from the manufacturer's data sheet plus about 150–200 V typical margin for general IGBTs. The breakdown voltage could also be measured with a curve tracer.

Besides the above simple but rough extraction method, the extrapolation based on the $C_{\rm oes}$ and $C_{\rm res}$ versus collector–emitter voltage curves in the datasheet can also lead to a reasonable extraction value of N_B using the analysis in [24] and [15]. This leads to a linear relationship between $1/(C_{\rm oes}-C_{\rm res})^2$ and $V_{\rm CE}$, shown in (14). The slope of this relationship, which may be obtained using linear regression performed on the datasheet curves, can be used to find N_B since the area A and intercell area ratio a_i are already known

$$\frac{1}{(C_{\rm oes}-C_{\rm res})^2} = \frac{2}{q\varepsilon N_B(A(1-a_i))^2}V_{\rm CE}. \tag{14}$$

The extraction of the drift region (base) width W_B is different for PT and NPT devices. The NPT has a triangular shape of electric field distribution, and it is designed to PT at the same voltage as avalanche breakdown.

Under the triangular shape of the electrical field distribution in the NPT IGBT, the breakdown voltage due to PT is

$$V_{\rm PT} = \frac{qN_B(W_B)^2}{2\varepsilon}. \tag{15}$$

For PT devices, where the electric field is trapezoidal, the breakdown voltage due to avalanche is

$$V_{\rm BR} = E_C W_B - \frac{qN_B}{2\varepsilon}W_B^2 \tag{16}$$

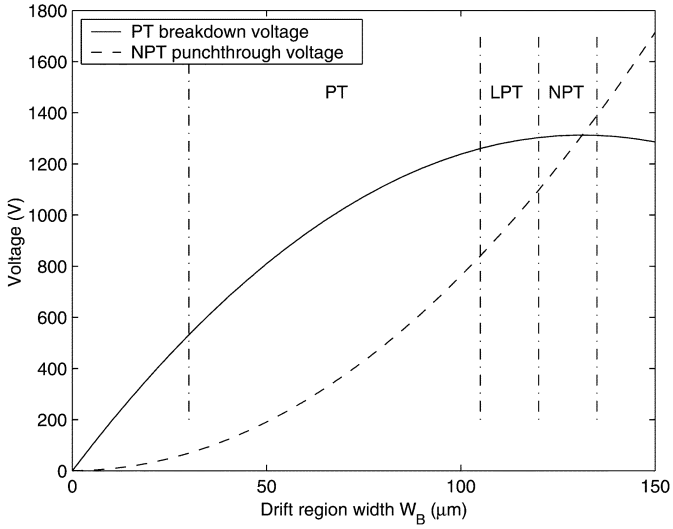

Fig. 8. PT and breakdown voltages as a function of drift region width for NPT, LPT (light PT), and PT structures, with $N_B = 1\times10^{14}$ cm^{-3}. The NPT, LPT, and PT regions are indicated in the figure.

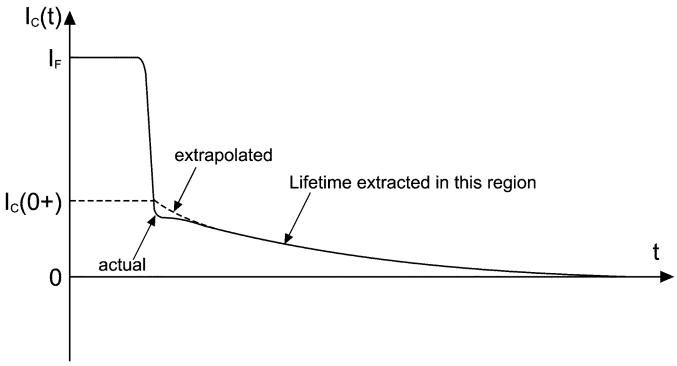

Fig. 9. IGBT current waveform under inductive turn off.

where E_C is the critical electrical field value for silicon ($E_C \approx 2\times10^5 - 3\times10^5$ V $\cdot$ cm^{-1}). Fig. 8 shows the curves of $V_{\rm BR}$ against drift region width W_B with a doping N_B of 1×10^{14} cm^{-3} for both NPT and PT structures. As can be seen from the figure this gives a maximum breakdown voltage of approximately 1330 V. The intersection of the two curves gives the width for which avalanche and PT occur for the same voltage, i.e., the width for which a NPT device would be designed. A PT design would typically have a drift region width less than this. The breakdown voltage advantage of the PT structure for the same drift region width can clearly be seen in the figure.

Hence this figure can be used to determine W_B and the likely structure. Solving the quadratic in (16) gives the following expressions for W_B:

$$W_B = \begin{cases} \frac{\varepsilon E_C}{qN_B} & \text{(NPT)} \\ \frac{\varepsilon}{qN_B}\left(E_C - \sqrt{E_C^2 - \frac{2qN_BV_{\rm BR}}{\varepsilon}}\right) & \text{(PT).} \end{cases} \tag{17}$$

4) IGBT Lifetime Parameters: Extraction of the high-level lifetime $\tau_{\rm HL}$, and, in the case of the PT structure, the buffer layer lifetime $\tau_{\rm BF}$, must be obtained from inductive turn-off measurements, specifically the current tail. This is shown in Fig. 9. The decay rate of the current tail is set by the lifetime.

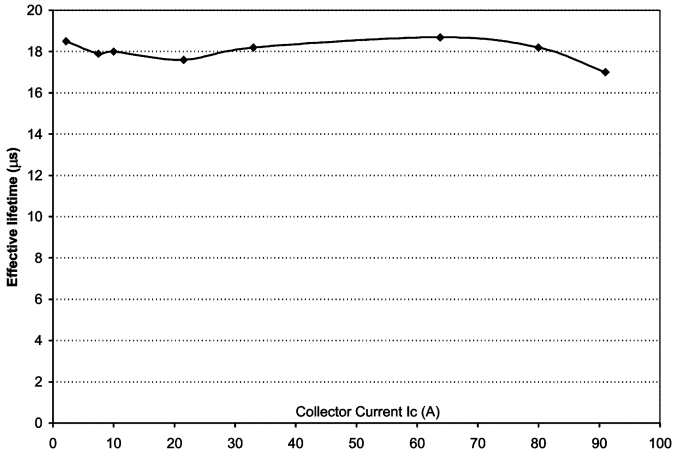

Fig. 10. High-level lifetime extraction for the *Dynex* NPT IGBT (the x-axis is collector current, 10 A/div, and the y-axis is time, 2 μs/div).

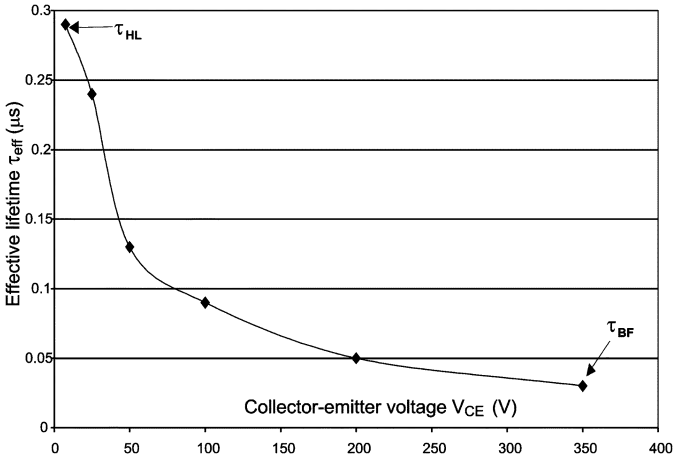

Fig. 11. Effective lifetime extraction under different clamped voltages for the PT IGBT (the x-axis is collector–emitter voltage, 50 V/div, and the y-axis is time 0.05 μ s/ div).

Based on the theory in [4], the IGBT current decay during the current tail for a constant collector voltage is given by

$$I_C(t) = \frac{I_C(0^+)}{\left\{\left[\frac{I_C(0^+)}{I_k^\tau}+1\right]\exp\left(\frac{t}{\tau_{\rm HL}}\right) - \frac{I_C(0^+)}{I_k^\tau}\right\}} \tag{18}$$

where $I_C(t)$ is the collector current, and I_k^τ is defined as

$$I_k^\tau \equiv \frac{q^2 A^2 D_p n_i^2}{I_{\rm sne}\tau_{\rm HL}}. \tag{19}$$

This expression can be approximated for $t > 2\tau_{\rm HL}$ as

$$I_C(t) \approx \frac{I_C(0^+)}{\left[\frac{I_C(0^+)}{I_k^\tau}+1\right]}\exp\left(-\frac{t}{\tau_{\rm HL}}\right). \tag{20}$$

Therefore, the high-level lifetime can be extracted by extracting the time constant of the exponential current decay a couple of time constants after the initial current fall time as shown in Fig. 9. It should be noted, that the accuracy of this method willl not be assured for IGBTs with lifetimes greater than approximately 10 μs due to the assumption of a linear charge profile made in [4]. However, this method will provide an initial estimate of the lifetime which can be refined either by hand or using the automated optimization described in Section V.

Fig. 10 shows the measured results of a *Dynex* NPT IGBT with a 90-A current rating. Notice that the effective lifetime is approximately independent of the collector current, therefore the collector current level used to extract the high-level lifetime is unimportant.

For the lifetime extraction of the PT IGBT, a method similar to the NPT case can be used. The difference is that the effective lifetime $\tau_{\rm eff}$, instead of the high-level lifetime $\tau_{\rm HL}$ in the NPT case, is used in (20) for the PT case. The effective lifetime is function of the high-level lifetime in the drift region and low-level lifetime in the buffer layer $\tau_{\rm BF}$ (equal to the minority (hole) lifetime τ_{pH}). Moreover, $\tau_{\rm eff}$ is dependent on the clamp voltage, unlike $\tau_{\rm HL}$ in the NPT case, which is independent of the voltage. Therefore, lifetime extraction for the PT IGBT needs to be performed under several clamp voltages. The effective lifetime extraction under clamp voltage condition is the same as in the NPT case. Fig. 11 shows the curve of the effective lifetime $\tau_{\rm eff}$ versus the clamp voltage based on the test results for a PT IGBT. Notice that Figs. 10 and 11 have different x-axes: in Fig. 11 the x-axis is the collector–emitter voltage, whereas in Fig. 10 the x-axis is the collector current. The high-level carrier lifetime $\tau_{\rm HL}$ corresponds to the low-voltage $\tau_{\rm eff}$ value, while the low-level carrier lifetime in the buffer layer $\tau_{\rm BF}$ is equal to the $\tau_{\rm eff}$ value at high clamp voltage since the drift region is depleted under that condition.

5) IGBT Recombination and Buffer Layer Parameters: The recombination parameter h_p (in the NPT case) and the buffer layer parameters N_H, W_H, and $I_{\rm sne}$ (in the PT case) set the level of injection from the P^+ emitter into the N^- drift region. The initial height of the current tail $I_C(0+)$ is set by the level of stored charge within the drift region, which is in turn set by the level of injection from the $P+$ emitter. Increasing h_p for the NPT IGBT, or increasing $I_{\rm sne}$, W_H or N_H for the PT IGBT, reduces the level of stored charge and therefore reduces the initial height $I_C(0+)$. Generally, a value of 1×10^{-12} cm^4 s^{-1} may be used for an initial estimate for h_p in the NPT case.

The remaining parameters of the buffer layer for PT IGBTs can be obtained based on their empirical value range. The typical PT IGBT buffer layer width W_H is about 4–10 μm. The normal range of the doping concentration N_H is 10^{16}–10^{17} cm^{-3}. For a relatively low-doped buffer region used in structures such as the CSTBT or field-stop (FS) IGBT, smaller W_H and N_H values should be chosen. In the PT model, $I_{\rm sne}$ is used instead of h_p and an empirical value of 10^{-14}–10^{-12} A may be chosen as an initial estimate. As for the NPT IGBT, the tail current height decreases with increasing values of $I_{\rm sne}$. Note that the hole diffusivity D_{pH} used in the PT model is reduced from its intrinsic value due to the high doping of the buffer layer, and therefore depends on the buffer layer doping N_H [26].

C. Initial Circuit Parameter Estimation

Estimation of the stray inductance L_S in the switching loop of the circuit is critical for modeling the switching process. It controls the slope of the reverse recovery current waveform in the case of the diode, and the current and voltage waveforms in

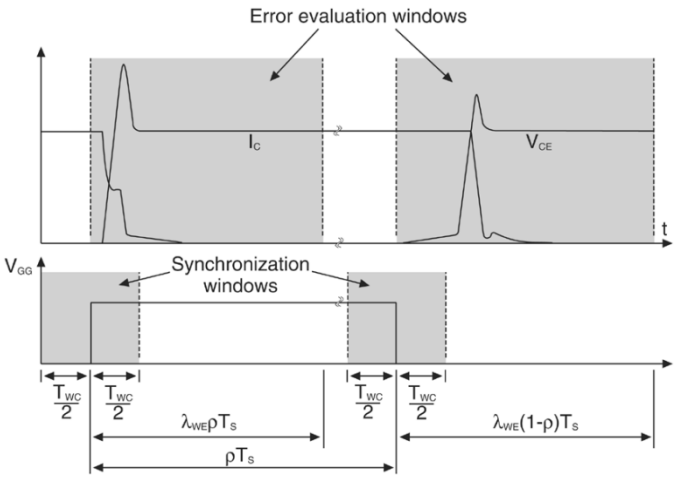

Fig. 12. Typical features of experimental waveforms. T_S: switching period, ρ: duty ratio, λ_{WE}: proportion of cycle used for waveform error evaluation, T_{WC}: length of window used for cross correlation (synchronization).

the case of IGBT switch-off. The diode reverse recovery waveforms are traditionally used to estimate the stray inductance

$$L_S = \frac{V_{\rm DC}}{\left|\frac{dI_A}{dt}\right|}. \tag{21}$$

A disadvantage with this method is that it assumes that the IGBT voltage $V_{\rm CE}$ is negligible, which is not necessarily true. A more accurate method would be to use the voltage dropped across the stray inductance, $V_{\rm DC} - V_{\rm CE}$. However, this suffers from nonconstant $V_{\rm CE}$ during turn-on, making the choice of point at which to estimate the stray inductance more difficult.

Therefore a more robust method is recommended for estimating L_S using the IGBT turn-off waveforms, since the diode voltage is negligible during this phase of the switching cycle (it is undergoing forward recovery)

$$L_S = \frac{V_{\rm CM} - V_{\rm DC}}{\left|\frac{dI_C}{dt}\right|}. \tag{22}$$

$V_{\rm CM}$ is the peak collector voltage during IGBT turn-off and $V_{\rm DC}$ is the supply voltage. The current slope dI_C/dt is measured during the initial current fall. It is also essential to include the Kelvin emitter inductance L_E (between the emitter terminal and the return path to the IGBT gate drive) in the simulation of the switching circuit, since this affects the shape of the IGBT collector voltage waveform during IGBT turn-on. This is typically 5–20 nH for a 1- cm^2 IGBT.

VI. Optimization Procedure

A. Experimental Measurement of Switching Waveforms

The optimization procedure requires suitable experimental waveforms from inductive switching tests to compare with the simulation waveforms. Ideally, these should be captured using a digital oscilloscope and transferred to the host computer, allowing a direct comparison with the simulation waveforms to produce an error figure which is then used to guide the optimization. The waveforms acquired for the tests described had the features shown in Fig. 12. A frame of 50 μs was captured at a sample rate of 200 MHz, giving 10^4 samples per frame. A switching "period" of $T_S = 40$ μs was included within this, incorporating both switching events, with the turn-on occurring 5 μs from the start of the frame. In addition to the extraction of IGBT parameters, these waveforms also allow the extraction of diode parameters from the diode reverse recovery current reflected in the IGBT turn-on waveform.

B. Waveform Evaluation

One possible method of comparison of the measured and simulated waveforms is using the salient points of the waveforms, e.g., diode reverse recovery current, reverse recovery time or IGBT switching time. This gives a small number of points to match, but can suffer from low accuracy. Most importantly, the waveforms may differ quite substantially during the switching instants, especially in di/dt and dv/dt. This would give a large error in estimated power during simulation. A much more accurate method of comparison is to simply calculate the sum of the squared errors at each time point in the waveforms. This requires the following.

- A method to compare the different traces of each waveform, typically voltage and current.
- Normalization of the errors used, so that the conditions imposed such as supply voltage and load current do not affect the consistency of the parameter extraction.
- Accurate synchronization of the waveforms, otherwise the errors in di/dt and dv/dt will be significant and lead to inaccuracy of the power loss estimates during simulation.

Accurate power loss estimation is the goal of the parameter extraction. One possible basis for the error is the instantaneous power dissipation. This encompasses the most critical points in matching the voltage and current traces, since maximum instantaneous power dissipation is usually where di/dt and dv/dt are high. Therefore, a possible waveform comparison method is to compute the sum of the squared errors at each time point of the instantaneous power dissipation. However there is the significant disadvantage of the independence of the voltage and current traces being lost when optimization takes place. For example, the same power dissipation waveform can be maintained by the voltage increasing and the current decreasing; while the power dissipations match, the voltage and current waveforms do not. Therefore the voltage and current waveforms should be used separately, and given that these are matched the power dissipations will match too. Matching voltage and current waveforms will tend to ensure that any oscillations, the waveform slopes and the switching energies are all matched. Normalization to the supply voltage and load current may be performed before the power dissipation is calculated, allowing comparisons between different operating conditions. Finally, summing the squared errors, rather than the magnitudes of the errors, assigns more significance to any large errors between measured and simulated waveforms. It has the effect of emphasizing the switching losses. This is useful since it forces the optimization to reduce the large errors first and converges quickly. The error figure used is therefore the sum of the normalized squared errors for the current and voltage at both turn-on and turn-off

$$f_e = SSE\left(\frac{V_{\rm CE,on}}{V_{\rm DC}}\right) + SSE\left(\frac{I_{\rm C,on}}{I_F}\right) + SSE\left(\frac{V_{\rm CE,off}}{V_{\rm DC}}\right) + SSE\left(\frac{I_{\rm C,off}}{I_F}\right) \tag{23}$$

$$SSE(x) = \sum_{n=1}^{N} (x_{\text{sim}}(n) - x_{\text{meas}}(n))^2 \quad (24)$$

where N is the number of samples in window.

Typically, synchronization is carried out "by eye," and matches both the time scales and the slopes (di/dt and dv/dt). A simple synchronization is to align the gate drive signals, which are available in both the hardware and the simulation used and are square waves [12]. An alternative is to compare the instantaneous power dissipations and find the relative delay of the waveforms which produces the minimum error between them, thus removing the effect of the gate drive circuit. This method was found to be the most effective. To perform the synchronization automatically, the cross correlation between the experimental and simulated traces is calculated. The cross correlation between two continuous signals $x(t)$ and $y(t)$ can be defined as

$$r_{xy}(\tau) = \int_{-\infty}^{+\infty} x(t+\tau)y^*(t)dt. \quad (25)$$

Here the waveforms are sampled, so the cross correlation for discrete signals $x(n)$ and $y(n)$ is used

$$c_{xy}[k] = \sum_{n=-\infty}^{+\infty} x(n+k)y^*(n). \quad (26)$$

If the waveforms are similar enough, which will be the case since the model is relatively accurate and the initial parameter set should give reasonable results, then the time delay τ or k at which the cross correlation is at a maximum equals that which will produce the best matching. The appropriate function in MATLAB is `xcorr`, which in this case is set to produce the unbiased estimate of the correlation

$$c_{\text{xy,unbiased}}[k] = \frac{1}{|N-k|} \sum_{n=0}^{N-k-1} x(n+k)y^*(n). \quad (27)$$

The correlation of the power dissipation waveforms uses a window of length $T_{WC}/2 = 4\ \mu$s either side of the gate step, to ensure that the switching event is captured. Once the matching delay is determined, the error between the waveforms can be calculated at each point, squared and summed to produce a single error estimate. The windows used for the error estimation are set to 50% ($\lambda_{WE} = 0.5$) of the on- or off-state period. In this case, the sum of these periods (T_S) is 40 μs. Refer to Fig. 12 for details. A summary of the simulation and waveform evaluation process is as follows.

1) Update the parameters to reflect the new point in the search space.
2) Simulate the switching cycle.
3) Obtain the waveforms from simulation and experiment. The simulation waveform may need to be interpolated to get a uniform sample rate. Also normalize the waveforms to the off-state voltage and on-state current (i.e., divide V_{CE} by V_{DC}, I_C by I_F).
4) Calculate the instantaneous power dissipation for each ($= V_{\text{CE}} \times I_C$).
5) Window two sections of each waveform: one around the turn-on event, one around turn-off.
6) Calculate the cross correlation of the windowed waveforms (MATLAB function `xcorr`).
7) Search for the maximum cross correlation (MATLAB function max).
8) Apply the shift (the number of samples to which the maximum cross correlation applies) to synchronize the waveforms for both turn-on and turn-off.
9) Re-window the shifted waveforms.
10) Subtract the simulated waveforms (V_{CE} and I_C for both turn-on and turn-off) from their experimental counterparts. Square the differences and sum them to give the sums of square errors (SSEs).
11) The error figure f_e equals the sum of the four SSEs.

C. Parameter Optimization

Optimization techniques rely on finding the minimum of an objective function (also known as a cost function). This is specific to a particular problem, and must be a function of the system parameters. The optimum set of parameter values will give the minimum objective function, which is in this case the error figure f_e between the measured and simulated waveforms.

Common optimization techniques used in power engineering, including the design of circuits, components and machines, are optimization by steepest descent or stochastic searches. Steepest descent, a traditional method of optimization, suffers from only being able to find a local minimum, not necessarily the global minimum, and is dependent on the start position. This can be ameliorated using additional heuristics such as a variant of the Tabu search [27]. Stochastic searches such as simulated annealing and genetic algorithms find the global minimum more effectively by introducing random parameter variation [28]. The advantage of using these is their complete and relatively quick search of the parameter space. However, this is only of benefit where the objective function is likely to be multimodal, i.e., contain many minima.

In the case of parameterization the starting point is likely to lead directly to the global minimum since the model is accurate and the initial parameter set should be a good estimate. Hence, a simple direct search, without additional heuristics, may be used. In addition, the search time must be kept reasonably low, particularly since the number of parameters is high, giving a large parameter space. Using genetic algorithms or simulated annealing would increase the search time prohibitively.

In the direct search [29], locating a minimum relies on the method of steepest descent. For analytic objective functions, the gradient can be calculated at any point. Frequently though, the objective function is not an analytic function of the parameters, and as this is the case here, the use of the direct search is dictated. Therefore, the objective function must be evaluated at points surrounding the current position in the parameter space.

The Hooke and Jeeves search [30] is a variant on the direct search. After evaluating the objective function at points surrounding the current (base) point, a move in a particular direction is made, and then a test is made to see if further movement in the same direction would give another reduction in the objective function. This is known as a *pattern move*, and can increase the speed at which the minimum is reached. It is particularly useful with a large number of parameters, where the cost of re-evaluating the space surrounding a particular point is high. A feature from the Tabu search is added, which ensures that points

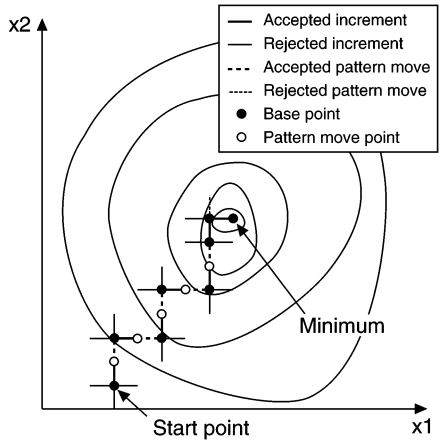

Fig. 13. Example of Hooke and Jeeves direct search with two variables.

visited recently (i.e., the last M base points) are not revisited. M is typically between 5 and 10 for small-scale problems (up to 12 parameters), and is set to 8 here. If the error figure does not improve on the global minimum within two base points, the search terminates. Finally, if the simulation suffers from convergence problems, including a time-out, where the number of time steps exceeds a specified limit, the waveform evaluation returns an objective value of infinity. This forces the optimization algorithm to ignore this point and continue searching in other directions. Fig. 13 shows a graphical example of the direct search with two variables.

A summary of the optimization process is as follows.

1) Start at initial (base) set of parameters, perform the simulation and obtain the error f_e (i.e., the objective function).
2) Simulate and evaluate the error at each surrounding point, i.e., $\pm\Delta x_i$ for each parameter x_i. This requires twice the number of evaluations as there are parameters.
3) Find the lowest (i.e., best) out of these, and move there. If this is lower than the base point, this becomes the new minimum and the new base point. If none are lower than the base point, the minimum has been found so the search is terminated.
4) Move in the same direction as the move to the new base point and re-simulate and evaluate the error (this is the pattern move). If the error is lower still, then this becomes the new base point and minimum.
5) Return to step 2), ensuring that previously visited points are not revisited (this feature from the Tabu search saves the execution time).

VII. Results

A. Validation of the IGBT Model and Parameter Extraction

In order to validate the analytical IGBT model and the initial parameter extraction method (step 1), the IGBT model with extracted parameters was used to simulate the switching behavior of various structure IGBTs from different manufacturers. They are listed in Table IV.

In order to avoid the effects introduced by the external circuit, the validation experiments were performed under a simple hard switching environment, including resistive and clamped inductive load test circuits. The current generation of IGBTs generally has very fast switching speeds and becomes sensitive to the circuit parameters; therefore these parameters, such as parasitic inductance, have to be precisely measured and accounted for in the simulation.

TABLE IV
IGBTs Tested

IGBT	Structure	Rating	Manufacturer
A	Trench PT	600V/600A	Powerex
B	DMOS PT	1200V/600A	Powerex
C	DMOS NPT	1200V/100A	Dynex
D	Trench Field Stop	1200V/80A	Infineon
E	DMOS NPT (with diode)	1700V/400A	Semikron

The comparison between the experimental and simulated results for various IGBTs at turn-off under clamped inductive load circuit is seen in Fig. 14(a), (b), and (d). Note that large snubbers across the diode and the IGBT were used in these tests as described in the figure captions. Resistive switching was used for the results shown in Fig. 14(c). The time scale is 200 ns per division. The simulations were carried out in PSpice.

B. Optimization of IGBT and Diode Parameters

IGBT E was tested in a clamped inductive load circuit. The initial parameter extraction (step 1) was used to obtain estimates of the parameters, a selection of which is shown in Table V.

Experimental waveforms for both turn-on and turn-off were obtained for several sets of conditions. The conditions varied were the load current I_F, the supply voltage $V_{\rm DC}$ and the on-state period $t_{\rm on} = \rho T_S$. Optimization of the parameters in Table V was performed for each set of conditions. The simulations were carried out in Simulink. The conditions, the resulting parameter variation and the percentage error reduction in total switching energy E_{SW} (relative to the experimental waveforms) are given in Table V. Each of the 12 parameter optimizations took an average of 21 min to run, using a Pentium IV machine with 512-MB RAM running Windows 2000. Each simulation lasted between 3 and 4 s, therefore requiring approximately 1 min for the search space around each base point to be evaluated with nine parameters.

Figs. 15 and 16 show the normalized voltage and current waveforms before and after optimization for test 1, Table V for turn-on and turn-off, respectively. The power dissipation waveforms are obtained by multiplying the voltage $(V_{\rm CE})$ and current (I_C) waveforms.

VIII. Discussion

The waveforms in Figs. 15 and 16 show that the optimization procedure improves the matching of both the device waveforms and the power dissipation during switching. The waveforms are shown after synchronization, with the start of the window $(t = 0\ \mu{\rm s})$ coincident with the appropriate edge of the simulation gate drive signal V_{GG}. The synchronization using the power dissipation for cross correlation produces well-aligned voltage and current waveforms.

The matching of experimental and simulated waveforms is particularly close during turn-off. The main source of error

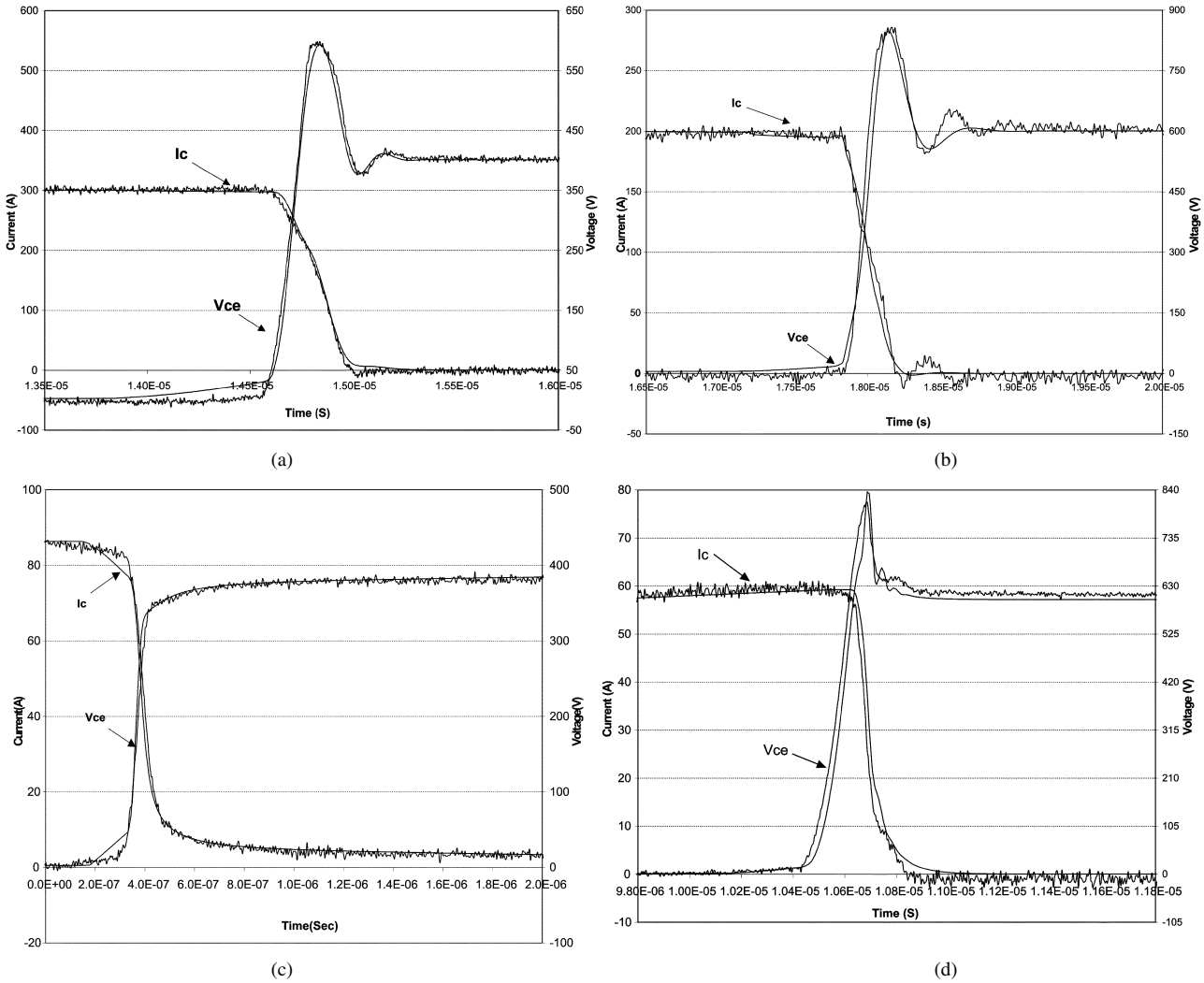

Fig. 14. (a). Comparison of experiment and simulation for IGBT A at turn off at 400 V/300 A (inductive switching). The IGBT had an R–C snubber of 3.4 $\Omega-9.4$ nF and the diode had an R-C snubber of 3.4 $\Omega-20$ nF. (b). Comparison of experiment and simulation for IGBT B at turn off at 600 V/200 A (inductive switching). The IGBT had an R–C snubber of 3.4 $\Omega-9.4$ nF and the diode had an R-C snubber of 3.4 $\Omega-5$ nF. (c). Comparison of experiment and simulation for IGBT C at turn off at 400 V/90 A (resistive switching). No snubber was used. (d). Comparison of experiment and simulation for IGBT D at turn off at 600 V/60 A (inductive switching). The IGBT had no snubber and the diode had an R–C snubber of 3.4 $\Omega-14$ nF.

isin the voltage $(V_{\rm CE})$ waveforms, where the voltage ramps during the gate plateau are too large. This is also visible in Fig. 14(a)–(c), and is being addressed in current work.

The results in Table V show that most parameters vary by up to approximately 25%. The diode and IGBT areas A, the diode lifetime $\tau_{\rm HL}$ and IGBT drift region width W_B only vary slightly from the initial set of parameters. This shows that both the initial parameter estimation is good and that the optimization is effective: indeed it recognizes that no significant refinement of these parameters is necessary. The switching energy errors decrease significantly in all optimizations, except for runs 8 and 9. This is because the devices have a long tail current, and the small error in current during the tail gives a large error in switching energy loss due to the integration end point timing. The choice of least squared errors between waveforms for the objective function results in a reduced sensitivity to this period of the switching waveform. Thus the estimated values of the IGBT carrier lifetime $\tau_{\rm HL}$ and the recombination parameter h_p can be expected to vary more widely than the other parameters. As no lifetime control is used in NPT IGBTs, a carrier lifetime of 100 μs is not unusual, as found in run 10, and the behavior of an IGBT under conventional switching is not greatly influenced unless very short lifetimes are used. A further issue arises associated with the absolute accuracy of the experimental current tail waveform, where an error will cause a poor estimate for h_p. Finally, in index 5 the simulated waveforms before optimization exhibit reduced convergence (while still completing simulation), giving a large turn-off energy loss. The waveforms after optimization do not show this, demonstrating the ability of the optimization to remove this discrepancy.

The diode reverse recovery clearly affects the IGBT current overshoot at turn-on. The current overshoot is an important contribution to the power dissipation of the IGBT, and as a result the diode parameters must be optimized in addition to those of the IGBT. This is an example of the coupled nature of IGBT and diode interaction in an inductive hard-switching environment, previously discussed in [17].

The validity of the model across the range of conditions chosen is good, shown by the low variation (up to 25%) of the parameter values. This emphasizes the accuracy of the model.

TABLE V
PARAMETER VALUES BEFORE AND AFTER OPTIMIZATION

Index	Conditions			IGBT					Diode		Circuit		E_{SW} error	
	V_{DC}	I_F	t_{on}	A	τ	W_B	N_B	h_p	A	τ	L_E	L_S	Before	After
Initial				4.0	6.7	200	6.7	5.0	4.0	0.30	1	400		
1	225	51	20	3.8	6.7	157	5.3	14.4	4.4	0.19	1	357	47	26
2	230	53	10	3.8	6.7	170	4.2	14.4	4.0	0.19	1	318	56	26
3	220	51	30	3.8	6.7	170	4.2	11.1	4.0	0.19	1	357	45	17
4	345	78	30	3.5	6.7	123	5.3	20.0	4.0	0.19	1	357	33	5
5	350	80	20	3.0	10.6	157	5.3	14.4	3.0	0.19	1.2	357	75	2
6	350	80	10	3.0	10.6	200	5.3	11.1	3.6	0.15	1	357	38	7
7	450	128	10	2.1	5.3	123	6.7	6.5	3.8	0.19	1	357	33	5
8	450	58	10	2.3	10.6	235	10.6	0.5	2.0	0.24	1	357	61	49
9	455	59	20	4.0	6.7	200	8.4	2.9	3.3	0.24	1	400	52	52
10	800	101	20	2.1	100.0	105	16.8	2.3	2.0	0.24	1	357	17	8
11	810	147	20	3.2	6.7	157	6.7	5.0	3.0	0.24	1	357	13	2
12	800	212	20	2.4	33.6	114	13.4	2.3	3.5	0.24	1	357	16	0
Units	V	A	µs	cm^2	µs	µm	10^{13} cm^{-3}	10^{-12} cm^4s^{-1}	cm^2	µs	nH	nH	%	%
Mean				3.1	17.6	159	7.7	8.7	3.4	0.21	1.0	357		
Standard deviation				0.7	25.9	37.6	3.8	6.0	0.7	0.03	0.1	17		
Std dev as % of mean				22	147	24	50	69	22	14	5	5		

It may be observed that the on-state period $t_{\rm on}$, associated with the duty ratio ρ, has no significant effect on the optimized parameter values. Therefore there is no need to vary this condition in practical parameter optimization. It is left to the user to choose representative operating conditions, having no practical impact on the optimization and resulting simulations, as would be expected for a robust and well-formed model. If several sets of conditions are used, taking the mean of the parameters across the conditions would be a suitable method of obtaining one set of parameter values.

A number of sets of conditions should be tested, over a wide range as illustrated in Table V, to obtain a set of final parameter estimates which are robust across a wide range of conditions. Achieving this avoids the danger of creating a set of parameters unique to particular conditions. Adopting the mean parameter values offers a practical approach. A parameter validity map [31] could be generated to indicate the matching of the experimental and simulated waveforms for different conditions, allowing designers to make informed decisions regarding the validity of the models. The conditions important in the application considered can be determined with the use of condition maps [32], which give the most likely sets of conditions for a particular load cycle. The use of these would allow the suitability of the models and parameters to be justified and point toward the suitable conditions under which the optimization of parameters should take place.

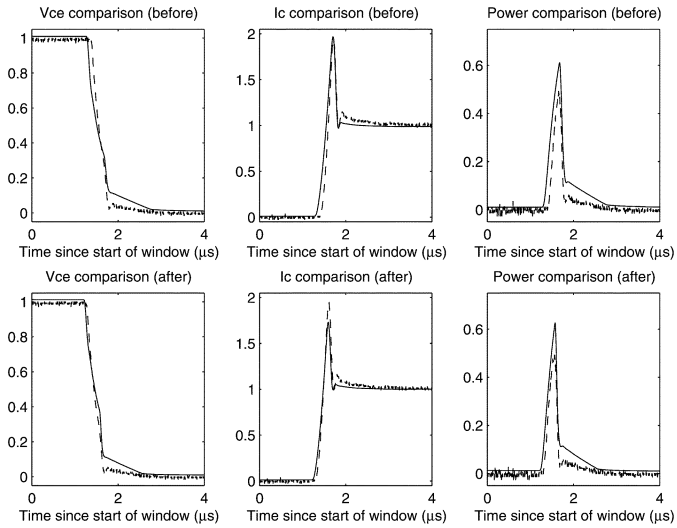

Fig. 15. Comparison of experimental waveforms (dashed) and simulated waveforms (solid) of IGBT turn-on before and after optimization for test 1 (IGBT E, 225 V, 51 A). Voltage and current traces are normalized relative to the supply voltage $V_{\rm DC}$ and load current I_F, and the power dissipation is normalized relative to $V_{\rm DC}I_F$.

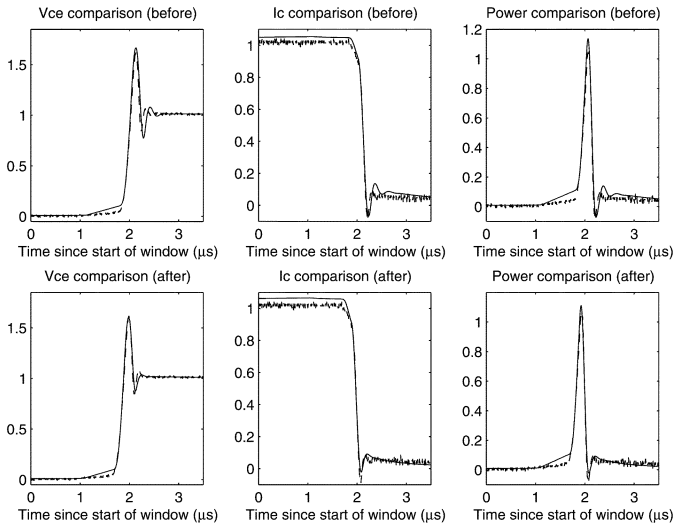

Fig. 16. Comparison of experimental waveforms (dashed) and simulated waveforms (solid) of IGBT turn-off before and after optimization for test 1 (IGBT E, 225 V, 51 A). Voltage and current traces are normalized relative to the supply voltage $V_{\rm DC}$ and load current I_F, and the power dissipation is normalized relative to $V_{\rm DC}I_F$.

IX. Conclusion

A practical parameter extraction method is provided for the FBS analytical IGBT model. Since the extraction procedure is general in nature, some methods used in the research are also suitable for the extraction of some parameters needed for other kinds of IGBT models. Once the parameter optimization is complete, the parameters may be used in models on any platform, including circuit simulators such as PSpice.

By jointly using three general parameter extraction methods —empirical value-based extraction, datasheet-based extrapolation, and simple test-based extraction—the total extraction procedure only needs a simple clamped inductive load test for the extraction of 12 and 15 parameters needed for the NPT and PT IGBT models respectively.

The validation with the experimental results from various structure IGBTs demonstrates the accuracy of the proposed IGBT model and the parameter extraction method. The combination of an initial parameter extraction and a parameter optimization procedure provides a solid foundation for automated parameter extraction. The use of MATLAB as a common environment allows simple implementation of the extraction procedure. The optimization results show a clear improvement in simulation accuracy from the initial parameter estimates. However, depending on the intended use of the simulation models, in some cases the accuracy obtained from the initial parameter extraction may be deemed sufficient, making the optimization step unnecessary.

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