Temperature Effects on Trench-Gate IGBTs

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***Abstract*- The switching characteristics (turn-on and turn-off) and forward conduction drop of trench-gate IGBTs are examined over a temperature range of -150 to 150 °C. An analytical description of the forward conduction voltage drop is presented based on temperature dependencies of the appropriate physical parameters and mechanisms. A physics-based PSpice model, incorporating much of the device behavior, is also described. Results from the model are compared to experimental waveforms and discrepancies are discussed.** [*]

I. Introduction

It is of interest to determine the switching and conduction properties of trench-gate IGBTs over extended ranges of operating temperature. As IGBTs become commonly used in increasing numbers in transportation applications and some niche areas, the understanding of their behavior, and appropriate modeling, over a wide range of operating temperatures is necessary. For example, automobiles are expected to increase in electrification such that by 2010, the amount of on-board processed power will be as high as 10 kW [1]. IGBTs are expected to be the dominant device for use in these power converters with junction operating temperature extremes ranging from –40 to 125°C. Other specialty areas such as large magnet power supplies use electronics operating in cryogenic environments [2].

There has been some information provided on trench-gate devices such as MOSFETs and 1200 V IGBTs [3]. This data illustrated advantages of the trench-gate technology over the older planar-gate devices. Some experimental and theoretical information has been provided for thyristors and first- and second-generation IGBTs functioning below 0°C [4-7], but little or no data exists for trench-gate IGBT devices operating over a wide temperature regime.

This paper presents experimental switching and forward conduction data as well as some theoretical discussions. The data are presented under ambient operating temperatures from –150 to 150°C. Switching experiments were performed using resistive loads to limit the device-circuit interaction.

Numerical models involving finite difference analysis generally offer the best accuracy in semiconductor device simulation. However, the computing time required is substantial and the underlying phenomena behind the device operation are not immediately apparent. Analytical or approximate models [8] are based on semiconductor physics. Equations representing physical behavior can be implemented in simulation software to give a fairly accurate representation of the device. The problems faced in generating an analytical model are devising the correct equations and determining the realistic boundary conditions while ensuring convergence of the model.

On the basis of good results gained modeling emerging devices [9], the Leturcq [10] method of solving the 1D charge profile is adopted in this paper. The boundary conditions needed for accurate modeling are developed. The necessary temperature dependent parameters and their implementation in PSpice are then described based on previous IGBT models [11]. Comparisons between the experimental and simulated waveforms are made and discrepancies are discussed.

II. IGBT Structure

Previous generation IGBTs have a punch-through structure designed around a p^+ Si substrate with two epitaxial regions (n^- drift region and n^+ buffer layer). Carrier lifetime reduction techniques are often used in the drift region to modify the turn-off characteristics. Recently, trench-gate devices have been designed with local lifetime control in the buffer layer [3]. High-voltage devices (>1.2 kV) have been created using a non-punch-through structure beginning with the n^- drift region as the substrate upon which a shallow (transparent) p^+ emitter is formed [12]. Cross-sections of typical unit-cells for planar-gate IGBTs are shown in Fig. 1.

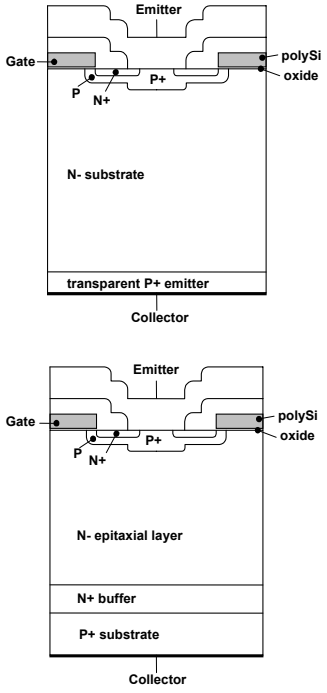

Fig. 1. Cross-section of a unit-cell in a high-voltage NPT IGBT (top), and a PT IGBT (bottom), each with the traditional planar gate.

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Third-generation IGBTs make use of improved cell density and shallow diffusion technologies that create fast switching devices with lower forward drops than have been achieved with previous devices. These lateral channel structures have nearly reached their limit for improvements. New trench-gate technologies offer the promise of greatly improved operation. Trench technologies can create an almost ideal IGBT structure because it connects in series the MOSFET and a p-n diode. There is no parasitic JFET as is created by the diffused p-wells in a lateral channel device (ref. Fig. 1). A simplified cross-section of the trench-gate IGBT is shown in Fig. 2. The forward drop in a trench-gate device is reduced significantly from the value in a third-generation lateral-gate IGBT. For example, in devices rated for 100 A and 1200 V, the forward drop, V_{CE}, is 1.8 V in a trench-gate IGBT as compared to 2.7 V in a lateral-gate (3rd generation) IGBT at the same current density, gate voltage, and temperature [3]. Local lifetime control is obtained in the n^+-buffer layer by using proton irradiation. This helps decrease the effective resistance in the n-base by increasing the on-state carrier concentration. The surface structure of the gate is such that the MOS-channel width is increased (causing a decrease in channel resistance).

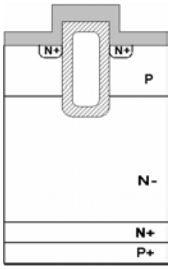

Fig. 2. Cross-section of a unit-cell in a PT IGBT using the trench-gate structure (not to scale).

III. IGBT Testing and Experimental Results

The IGBTs tested have maximum ratings as given in Table I below. The experiments were performed at several temperatures from –150 to 150 °C in increments of 50 °C. This set of testing was repeated three times, with three different resistive load values of 4, 2 and 1 Ω, corresponding to collector currents of 100, 200 and 400 A, respectively. The collector-emitter voltage was fixed at 400 V for each switching measurement. The amount of time that the IGBT conducts was variable from 10 µs, when the switching measurements were performed, to 500 µs for the forward voltage drop measurements. A diode clamp circuit was placed in shunt across the IGBT under test during the forward drop measurements to allow for increased resolution of the measurement.

TABLE I
Maximum Ratings

Symbol	Rating
V_{CES}	600 V
I_C	600 A
I_{CM}	1200 A

Figures 3 ,4, and 5 show the current fall during turn-off over the temperature range of –150 to 150 °C at collector current values of 100, 190, and 390 A, respectively.

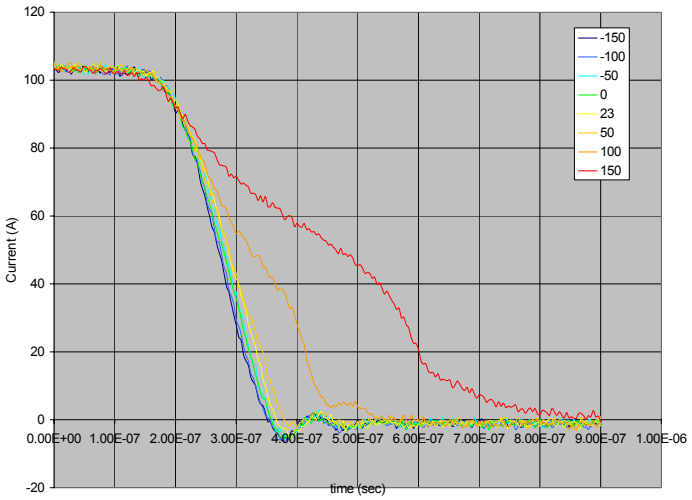

Fig. 3. Collector current fall during turn-off at temperatures from –150 to 150 °C. The peak current is 100 A and is switched off into a resistive load at 400 V. The horizontal scale is 100 ns/div.

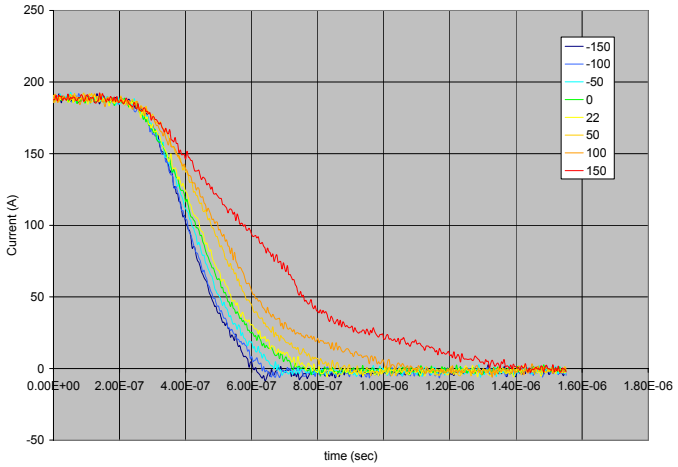

Fig. 4. Collector current fall during turn-off at temperatures from –150 to 150 °C. The peak current is 190 A and is switched off into a resistive load at 400 V. The horizontal scale is 200 ns/div.

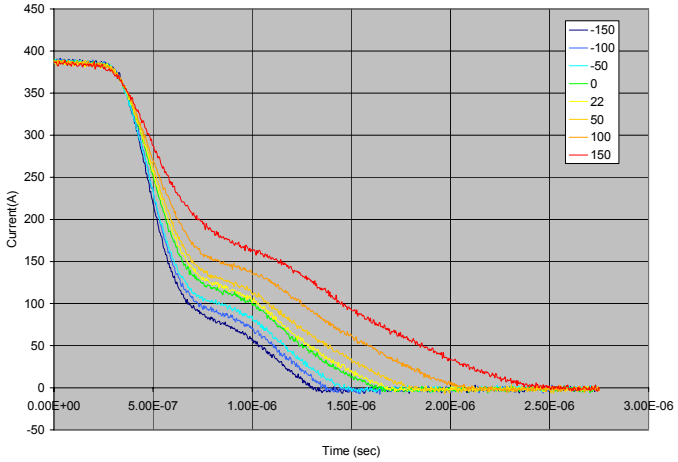

Fig. 5. Collector current fall during turn-off at temperatures from –150 to 150 °C. The peak current is 390 A and is switched off into a resistive load at 400 V. The horizontal scale is 500 ns/div.

The current waveforms show typical IGBT turn-off behavior except at junction temperatures of 100 and 150 °C (Figs. 3 and 4). These particular waveforms indicate initial turn-off of the MOS-channel followed by a short yet fast current fall, then ending in the traditional current tail during turn-off. At high collector current values (Fig. 5) the turn-off is consistent throughout the entire temperature range. The long tail-current section is probably due to the lack of hole injection across the buffer layer into the n-base so that recombination is slowed. The fall time (90-10% of peak current) at 150 °C increases from 500 ns to 1.7 µs as the current (and associated stored charge) increases from 100 to 390 A, respectively.

Figures 6 and 7 indicate the turn-off and turn-on energy losses, respectively, over the temperature range from –150 to 150 °C at three current levels.

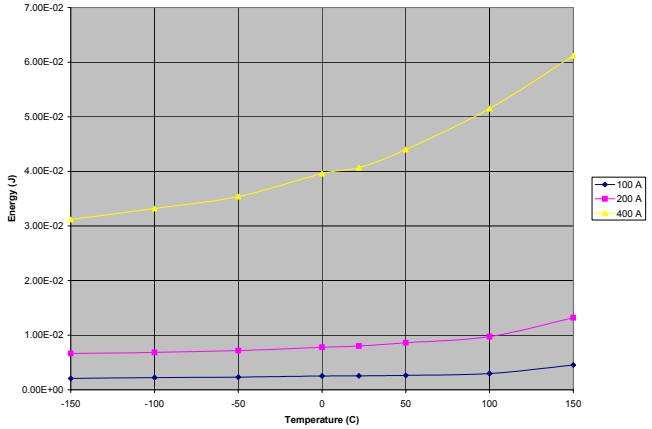

Fig. 6. Turn-off energy losses as a function of temperature for three values of collector current.

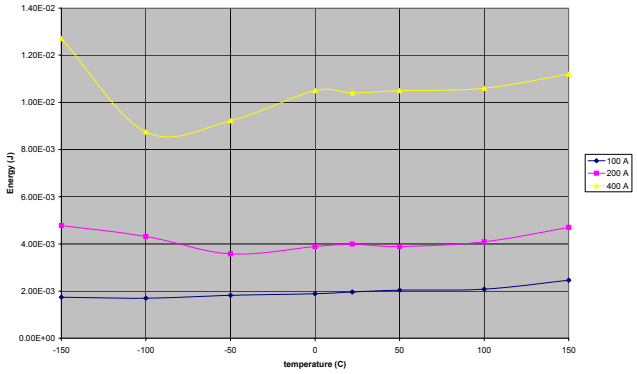

Fig. 7. Turn-on energy losses as a function of temperature for three values of collector current.

The turn-off losses increase as the temperature increases, as expected [11]. At low temperatures the turn-off time varies slightly so the associated losses are only weakly dependent on temperature. There is very little change in the turn-on losses over the temperature range examined. These two figures suggest that intentional cooling of the Si below 0 °C provides only marginally better performance if the switching losses dominate in the circuit application.

The forward voltage drop, V_{CE}, measured at various temperatures is shown in Fig. 8. It is clear from the curves (measured at 100, 200, and 400 A nominal) that above 0 °C the trend is for V_{CE} to decrease as the temperature increases. Clearly this behavior should cause some concern for parallel applications of these IGBTs, particularly in multi-chip modules.

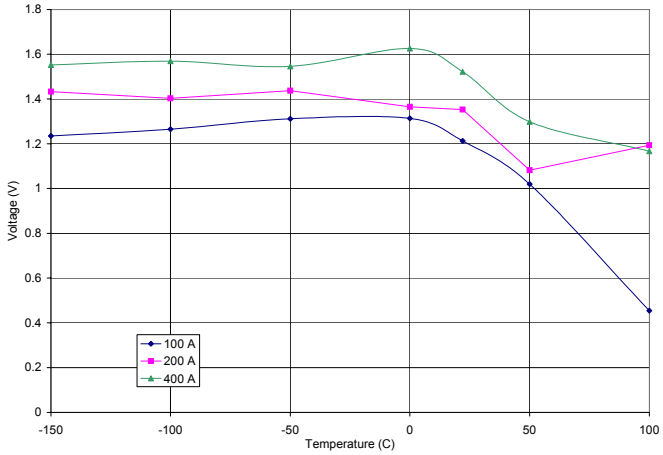

Fig. 8. Forward voltage drop in the on-state over a temperature range from –150 to 100 °C. The voltage is measured for I_C values of 100, 200, and 400 A.

IV. Model Development

A. Simulation of the Distributed Charge

The behavior of conductivity modulated devices, such as diodes and IGBTs, depends heavily on the excess carrier (charge) distribution in the wide drift region. In modern IGBTs, the charge profile has a 1D form over about 90% of its volume [11]. Thus, a 1D solution is adequate for the bulk of the device. Space-charge neutrality is maintained with the majority carrier profile closely matching the minority carrier profile (quasi-neutrality). Under these conditions, assuming high-level injection, the charge dynamics are described by the ambipolar diffusion equation (1):

$$D\frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{\tau} + \frac{\partial p(x,t)}{\partial t}, \qquad (1)$$

where D is the ambipolar diffusion coefficient, τ is the high-level carrier lifetime within the drift region and $p(x,t)$ is the excess carrier concentration. A Fourier based solution for this equation was proposed by [10]. The representation requires the width of the undepleted region and the hole and electron currents at the boundaries of the region (x_1 and x_2), which give the gradients of the carrier concentrations, $f(t)$ and $g(t)$ at x_1 and x_2, respectively. The functions $f(t)$ and $g(t)$ are defined by (2) and (3) as follows:

$$f(t) = \left[\frac{\partial p(x,t)}{\partial t}\right]_{x_1} = \frac{1}{2qA}\left[\frac{I_{n_1}}{D_n} - \frac{I_{p_1}}{D_p}\right] \qquad (2)$$

$$g(t) = \left[\frac{\partial p(x,t)}{\partial t}\right]_{x_2} = \frac{1}{2qA}\left[\frac{I_{n_2}}{D_n} - \frac{I_{p_2}}{D_p}\right] \qquad (3)$$

A is the cross-sectional area of the device, D_n and D_p, the electron and hole diffusion coefficients, I_{n1} and I_{p1} the electron and hole currents at $x = x_1$ (p^+ side), and I_{n2} and I_{p2} the electron and hole currents at $x = x_2$ (p-body side). A schematic of the n-base region where the ambipolar diffusion equation is solved using boundary current from (2) and (3) is shown in Fig. 9. Clearly, the success of the approach now depends solely upon developing the boundary conditions, especially those related to the effects near the MOS-source diffusion (n^+) and the p-body region in the device.

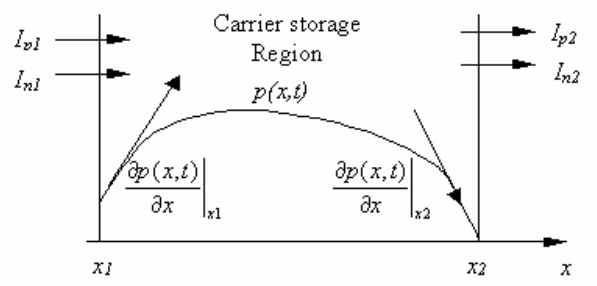

Fig. 9. Undepleted n-base showing stored charge and boundary currents.

The model developed is primarily concerned with accurately capturing the physical behavior of the stored charge in the n-base and the parasitic capacitances around the MOS-channel and the depletion region around the p-body and n-base. The electrical equivalent circuit representing Fourier terms for the stored charge is illustrated in Fig. 10.

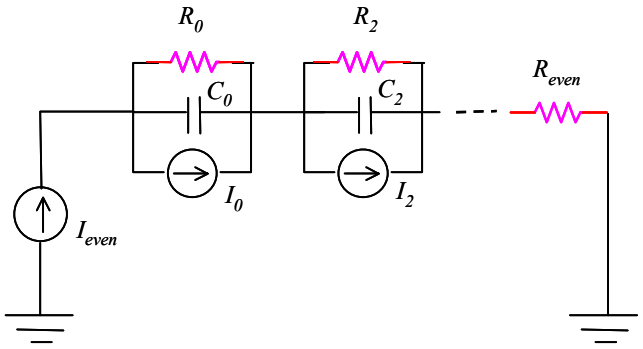

Fig. 10. Electrical equivalent circuit modeling the stored charge in the n-base (even harmonics of the Fourier series solution of the ambipolar diffusion equation).

The terminating resistor, R_{even}, is the sum of resistance of all the missing terms not included in the truncated series expansion. The shunt current sources are for moving boundaries of drift region, and the driving current, I_{even}= $D[g(t)$-$f(t)]$ is the current entering the IGBT unit-cell.

The current sources define the boundary conditions. The IGBT then appears as a controlled voltage source to the load in the circuit simulator. This controlled voltage source is made up of the junction drop across the p-emitter (IGBT collector) to n-base, V_{J1}, drop across the stored charge region, V_b, and the drop across the depletion region around the p-base/n-base junction, V_d. These simulate the main current path through the IGBT (collector current). The n-buffer region is ignored as a first approximation, but will be required in future simulations to capture this region's effects.

The forward drop, V_{CE}, is given by (4):

$$V_{J1} + V_b + V_d = V_{CE} \tag{4}$$

where

$$V_{J_1} = \frac{kT}{q}\ln\left(\frac{p_{x_1}p_{x_2}}{n_i^2}\right) \tag{5}$$

$$V_b = \frac{I_C}{\mu A q}\int_{x_1}^{x_2}\frac{dx}{p(x,t)} \tag{6}$$

$$V_d = \frac{q}{2\varepsilon_{Si}}\left(N_B + \frac{I_C}{qAv_{sat}}\right)W_d^2 \tag{7}$$

and

$$p(x,t) = p_0(t) + \sum_{k'=1}^{\infty} p_{k'}(t)\cos\left[\frac{k'\pi(x-x_1)}{x_2-x_1}\right] \tag{8}$$

In (6) A refers to the Si area, μ is the effective mobility given as the sum of the hole and electron mobilities, while in (7) N_B is the n-base doping concentration, v_{sat} is the saturation drift velocity, and W_d is the depletion width around the n-base/p-body junction. In (8) the Fourier series coefficients, $p_{k'}(t)$, form the R_nC_n components as shown in Fig. 10.

B. Temperature Dependent Parameters

Several dominant physical parameters associated with semiconductor devices are sensitive to temperature variations; causing their dependent device characteristics to change dramatically. The most important of these parameters are: *i*) the minority carrier lifetimes (which control the high-level injection lifetimes), *ii*) the hole and electron mobilities, *iii*) the free-carrier concentrations (primarily the ionized impurity-atom concentration), and *iv*) the intrinsic carrier concentration value, n_i. Almost all of the impurity atoms are assumed to be ionized at temperatures above 120 K (-150 °C) and are considered to be the impurity doping concentration values in the analysis.

Many empirical temperature dependencies of the carrier mobilities and recombination lifetimes are described in the literature [13-20].

The n- drift region in an IGBT is under high-level injection conditions during forward conduction and as such, recombination events there are described by the effective high-level carrier lifetime, τ_{HL}. A relationship for the temperature dependence of the carrier lifetime used in the simulations is given in (9). The values of the pre-factor and the temperature exponent in (9) will vary slightly depending on the details of device fabrication and design. The high-level lifetime is given in seconds and the temperature in Kelvin.

$$\tau_{HL} = 5\times10^{-7}\left(\frac{T}{300}\right)^{1.5} \tag{9}$$

The empirical relations used in the simulations, for electron and hole mobility as a function of temperature, are given by (10) and (11), respectively (T in Kelvin and μ in $cm^2/V\bullet s$).

Carrier-carrier scattering effects are not included in the equations, but will be in future simulation results.

$$\mu_n = 1400\left(\frac{300}{T}\right)^{2.5} \tag{10}$$

$$\mu_p = 450\left(\frac{300}{T}\right)^{2.5} \tag{11}$$

The intrinsic carrier concentration, n_i, appears as a parameter in the simulation equations as well, and its temperature dependence is given by [21] in (12).

$$n_i = \frac{3.88\times10^{16}(T)^{1.5}}{\exp\left(\frac{7000}{T}\right)} \tag{12}$$

It is a fair approximation for doping concentrations less than 10^{17} cm^{-3}. A more accurate expression for n_i that includes the temperature effects on the hole and electron density-of-states effective masses, bandgap narrowing, and a more exact solution to the Fermi integral, will all be included in future simulation results.

The IGBT has two further parameters which are affected by temperature: the MOS-gate threshold voltage and MOS-channel transconductance. These are approximated by:

$$V_{th} = V_{th0} - 9\times10^{-3}(T-300) \tag{13}$$

$$K_p = K_{p0}\left(\frac{300}{T}\right)^{0.8} \tag{14}$$

where V_{th0} is the device threshold voltage at 300 K and where K_{p0} is the transconductance at 300 K. The actual temperature during operation is determined using an equivalent electrical circuit as discussed by [22] and as shown in Fig. 11.

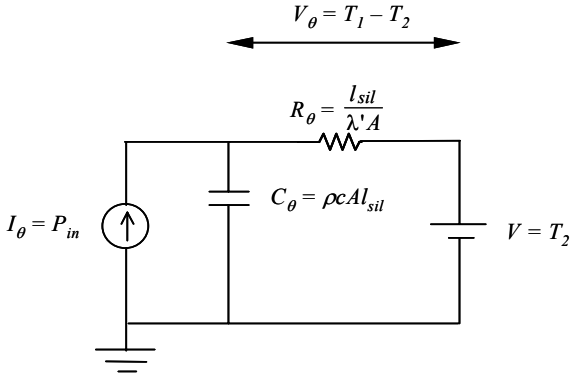

Fig. 11. Equivalent electrical circuit used for thermal modeling.

The temperature calculated from the thermal equivalent circuit is used to update the device parameters (9)-(14), which are used in turn to calculate the new value of carrier concentration and voltage drops across the IGBT, ultimately calculating the terminal voltages and currents through the PSpice model.

C. PSpice Simulation Results

The PSpice model has been highly developed for lateral gate IGBTs and has been shown to be fairly accurate [11]. An example of the model's high degree of accuracy is illustrated in Fig. 12 (simulated current-fall, voltage-rise and gate-voltage waveforms are delayed by about 40 ns from the experimental results). Therefore, there is obvious merit to adapting this model for the particulars related to trench-gate IGBTs.

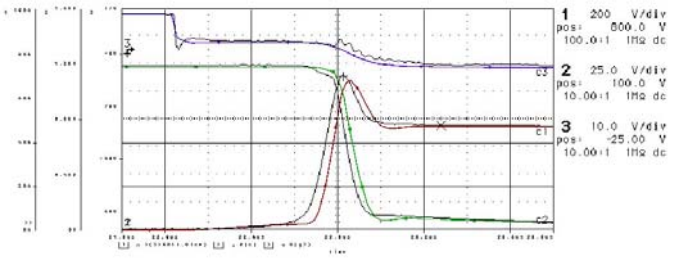

Fig. 12. Comparison of the PSpice model and experimental results for lateral gate IGBTs indicating overall model accuracy.

The simulation results are compared to the experimental turn-on and turn-off waveforms at room temperature and at 150 °C. The turn-on waveforms are shown in Figs. 13 and 14 (300 and 425 K, respectively). The turn-off waveforms are shown in Figs. 15 and 16 (300 and 425 K, respectively).

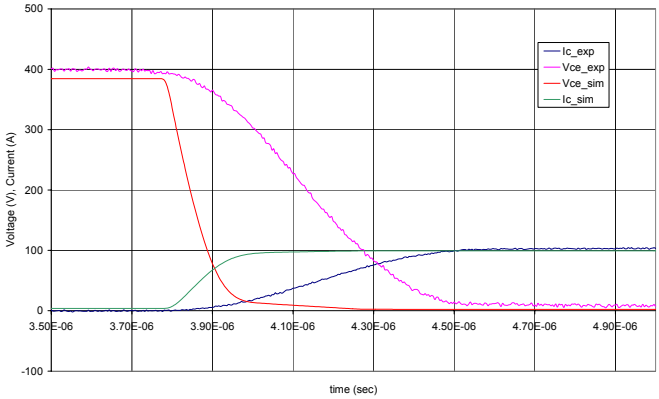

Fig. 13. Current rise and voltage fall during turn-on at 300 K comparing simulated (left-most) and experimental (right-most) waveforms. The horizontal scale is 200 ns/div. The current scale is in Amperes and the voltage scale is in Volts.

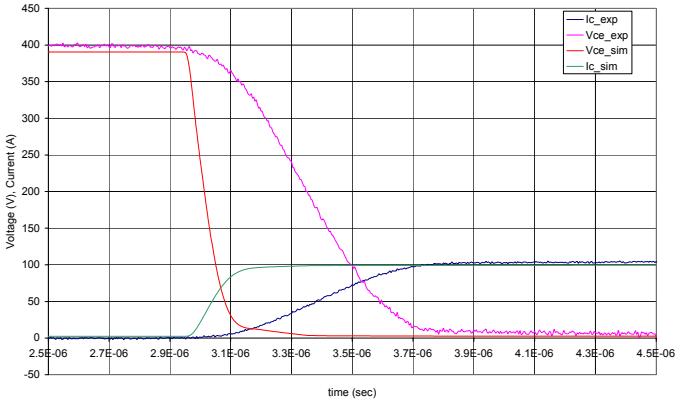

Fig. 14. Current rise and voltage fall during turn-on at 425 K comparing simulated (left-most) and experimental (right-most) waveforms. The horizontal scale is 200 ns/div. The current scale is in Amperes and the voltage scale is in Volts.

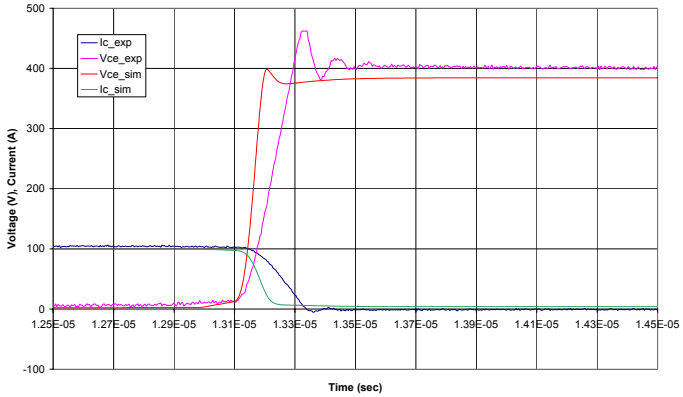

Fig. 15. Current fall and voltage rise during turn-off at 300 K comparing simulated (left-most) and experimental (right-most) waveforms. The horizontal scale is 200 ns/div. The current scale is in Amperes and the voltage scale is in Volts.

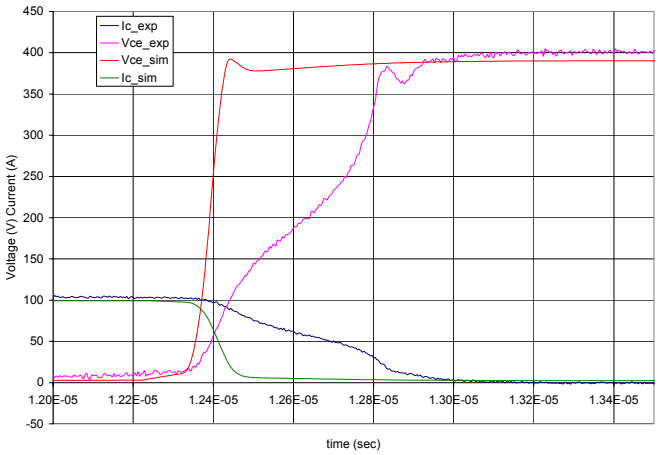

Fig. 16. Current fall and voltage rise during turn-off at 425 K comparing simulated (left-most) and experimental (right-most) waveforms. The horizontal scale is 200 ns/div. The current scale is in Amperes and the voltage scale is in Volts.

The simulated waveforms have transition times that are too short compared to the experimental waveforms. This is an indication of the need to more accurately model the gate-collector capacitance. The importance of this capacitance was noted in [11]. It is obvious that care must be taken in dealing with the geometry changes that are implemented in the trench-gate device as compared to the lateral-gate IGBT by noting the differences in simulation accuracy between Figs. 12 and 15.

The buffer layer and its associated lifetime control processing also appear in the experimental turn-off waveforms and are not considered as yet in the model physics. The exclusion of these influences are indicated in the too smooth shape of the simulated turn-off voltage and current waveforms in Figs. 15 and 16.

V. Discussion and Conclusions

The behavior of the Trench-gate IGBTs indicates the improved on-state drop compared to lateral-gate IGBTs. In addition, the buffer layer clearly has a significant affect on the switching dynamics.

As a result of only employing well-established physical models, it is possible to implement the electro-thermal conditions directly, again using well-established formulae. This allows the user to interpret the simulation results and gives a high degree of confidence in the results regardless of the operating conditions. The model developed for the lateral-gate structure is robust and highly accurate. Parameters needed for this model are the device geometry, n-base doping concentration, and carrier lifetime.

The understanding of the p^+-n^+ junction behavior and capturing that behavior in the trench-gate model is critical to improving the device simulation. Also, it is expected that the temperature dependence of the device model will be improved with better approximations to the parameters as described in (9)-(14). In these trench-gate devices the spatial dependence of the carrier lifetime is not appropriately taken into account, either. It is expected that improved versions of this modeling technique will include such in the future.

In general, IGBT modeling must be closely coupled with converter circuit operation, including the gate drive and free-wheeling diode operation. The gate-collector capacitance and stray inductance are important to accurately model IGBTs, particularly in modules. Further work is required to establish some paramaterisation principles. Finally, the fast computer run times are consistent with the use of such a detailed model in circuit simulation and therefore merit continued effort for improvement to increase the model accuracy.

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