Power sequencing approach to fault isolation in dc systems:
Influence of system parameters

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Abstract -- We show that medium-voltage dc power buses can be protected against short circuit faults by coordinating the action of a converter that supplies power to the bus with the action of contactors that are used to reconfigure the bus connections. Following a fault, the bus is de-energized (so there is no large current to interrupt), one or more contactors are reconfigured, and the dc bus is then reenergized. For a typical industrial dc bus, we show that it is possible to execute this de-energize-reconfigure-re-energize process 10 times faster than an AC bus can be protected and reconfigured using traditional circuit breakers. We show how the de-energizing and reconfiguring times depend on the output capacitance of the main converter and on the distance to the fault, and we show how to size each hold-up capacitor so that loads on unfaulted circuits can ride through the process uninterrupted.

Index Terms—MVDC systems, power electronics, fault protection, power sequencing, converters control.

INTRODUCTION
The increasing performance, higher efficiency, and decreasing cost of power electronic converters have spurred a rediscovery and proliferation of dc distribution systems [1, 2]. But still, protection of dc distribution systems against short circuit faults, especially at the medium-voltage level, is widely perceived to be a significant challenge because of the high magnitude of the fault currents [3, 4] and the lack of zero crossings in the current.

Common ac fault protector methods are not readily applicable to dc fault protection. Alternating currents naturally cross zero at every half-period, thereby creating conditions for self-extinguishing of currents in mechanical circuit breakers. In a dc system, there is no such natural zero crossing and currents must be forced to zero by external means before mechanical switches can be opened. [5]. In addition, the magnitude of a fault current might be quite large, being limited only by the resistance of the system (which is usually very low in order to permit low transmission losses), rather than by inductive impedance as in ac systems.

In this paper, we solve the widely-cited problem of arc extinction in the absence of periodic zero crossings of the fault current by coordinating the behavior of power converters with that of mechanical bus tie switches. The ultimate benefits of the proposed solution are twofold - traditional circuit protection elements such as circuit breakers are eliminated, and loads on un-faulted branches can ride through the rapid reconfiguration period.

Our new approach relies on a carefully timed sequencing of power converter settings and network switch reconfigurations. After a fault on a branch of the power network is identified, the following sequence of events occurs:

1) The main converter is turned off (i.e. the output voltage is set to zero)
2) When the fault current decays to a suitably small value, contactors are operated to isolate the faulted branch of the circuit and any other contactors that must be reconfigured are so operated.
3) The bus is re-energized.

Fig. 1 shows a simple system such as we are describing. If this were protected only by conventional means, large and not-yet-proven circuit breakers would have to be placed at all of the locations shown in the figure. In addition to these circuit breakers, many such systems would also contain mechanical disconnects that permit shutting off of individual branch circuits. Our approach eliminates all of the circuit breakers that are shown in Figure 1.
Fig. 1. All of the circuit breakers show in this system can be eliminated by use of the controlled power sequencing approach.

By operating the protection system quickly — within a few milliseconds – we permit rapid isolation of the faulty branch and rapid re-energizing of the entire bus such that loads on the healthy branches are not aware that the main bus has been brought down and reconfigured [6]. The elimination of traditional circuit breakers and the absence of additional hardware to protect the distribution system are significant advantages of this protection scheme. The contactors should generally be part of the system anyway, as they are used to isolate individual branches for maintenance.

Fig. 2. Overview of the power sequencing process.

Figure 2 shows the current waveforms associated with this controlled power sequencing approach. The red dotted waveform shows how rapidly the system can be reconfigured and power can be restored to an unfaulted branch of the system, whereas the solid line shows the longer time that would be needed to recover system operation if the controlled sequencing were not used. This example illustrates what happens when a line to ground fault occurs in the cable serving load 3. As described in detail in [6], the system bus current transients exhibit two distinct behaviors, as illustrated in Figure 2: the solid line shows the current after the identification of the fault and shutting off of the main converter; the dashed curve shows the additional benefit of the controlled power sequencing process. During time interval $t_1$, the current increases rapidly as the energy stored in the output capacitor of the main power converter is discharged. After this rapid discharge, during time interval $t_2$, the current decays more slowly, as the filter inductor of the main converter is discharged.

The current spike during interval $t_1$ can be destructive and poses the biggest challenge for the protection design. Two important features of the proposed protection scheme are (1) the reduction of this current spike by distributing the filter capacitance within the system and by isolating parts of this distributed capacitance through diodes, as shown in Figure 1; and (2) the coordinating control for the main converter that immediately suppresses power delivery when a fault is identified. The output capacitor of the main converter can be selected in such a way that the peak of the bus fault current will not exceed the rated current of the components.

If a fault occurs in branch 3, as shown in Fig 1, the protection system operates as follows: first, the fault is identified and the main converter is turned off; next, the energy accumulated in the output capacitor of the main converter is dissipated, and the fault current becomes equal to the current of the main converter’s inductor $L_{out}$; finally, once the fault current drops below the rated opening current of the contactor 3, the contactor 3 opens and the fault is isolated.

When compared to three traditional types of protection systems: ac-side protection; protection by direct interruption of the fault current; and protection by inducing an oscillating current, it is apparent that the proposed protection provides distinct benefits.

Traditional techniques for protecting dc systems [7, 8] induce an oscillating current to produce a current zero, and thereby to permit the interruption of the fault current in mechanical switches. Such techniques require additional components such as switches, charging or discharging capacitors, pre-charging circuits and power supplies. In contrast, the proposed solution does not require additional circuits for interrupting the fault current. What is more, it eliminates the need not only for any additional equipment but for current breakers as well.

Another common approach for protecting against dc bus faults is to operate the ac-side switches in crowbar mode, thus shorting and tripping an ac circuit breaker on the input side. But shorting the ac input may over-stress the power switches, and this approach can only be used when power is supplied from an ac bus, not if power is supplied from a dc bus.

Another solution is to use solid state circuit breakers (SSCBs) on the dc side. These are composed of a semiconductor switch, such as an IGBT or IGCT or ETO thyristor, and a snubber circuit that can include some combination of resistors, capacitors, and metal oxide varistors
Thanks to recent developments, SSCBs can quickly interrupt fault currents [9]. While the development of these devices is becoming more and more interesting, still some drawbacks exist. First, the current can never be allowed to exceed the maximum rating of the particular semiconductor device, else the device itself will fail. Secondly, the forward voltage drop of the semiconductor device during normal operation may be so much larger than that of a mechanical contactor that the power loss and thermal management become important issues.

**DC SYSTEM DESCRIPTION AND FAULT DYNAMICS**

Figure 3 shows a particular system that has been explored in simulations to prove out this concept. A main dc/dc converter supplies power to a dc distribution bus that supplies many branch circuits. The system we simulated is a 1 kV, 1 MW system. Switches SW1, SW2, and SW3 can be closed to supply power to the branch circuits, or they can be opened to isolate a branch circuit, but they are not capable of interrupting fault currents. When a fault happens, the loads on healthy lines are isolated by the input diodes while they draw power from the hold-up capacitors. Therefore, healthy load converters on healthy lines are able to supply power to each load for a time depending on the size of the load hold-up capacitors. For simplicity regarding system stability, our simulations assumed that loads on healthy lines had only a resistive characteristic. For simulations regarding the feeding of loads from hold-up capacitor, we used constant power load models to simulate controlled dc/dc converters that supply loads.

![Figure 3. Scheme of the dc bus used for the analysis](image)

The converter control, the output capacitor ($C_{OUT}$) of the main converter and its protection, input diodes, downstream input capacitors and branch switches are all involved in this process.

We have studied the performance of this system, and how the performance depends on system parameters. From this study, we have developed an understanding of the control sequencing and how the sequencing and the overall system performance are affected by component and system parameters.

![Figure 4. Current of the faulted branch (branch 3 in Figure 3)](image)

![Figure 5. Current of one of the unfaulted branches (branch 1 in Figure 3)](image)

Figure 4 and Figure 5 show the behaviors of currents in the faulty branch and in one of the unfaulted branches respectively. A line-to-ground fault happens at $t=0.011$ s. After detecting the fault at time point 1 the control turns off the main converter and, at time point 2, it isolates the faulted circuit by means of SW3 as soon as the current falls under the rated opening current of the contactor. The detection of the fault has been performed by simply measurement of the current on the branches.

![Figure 6. Voltage of the faulty branch](image)
Figure 6 shows the voltage on the faulty line, which drops to zero when a ground fault happens, while Figure 7 illustrates the comparison between the voltage of the faulted branch and the voltage of the main bus. Figure 8 shows that the voltage at a load served by a healthy line does not drop immediately but drops instead at a rate that depends on the size of the local hold-up capacitor and the power demand of the load. In this simulation the voltage on the load has the same behavior of the load current because of the resistive characteristic of the load. As soon as the fault is eliminated, the re-energizing process begins ($t = 0.0125$ s).

Figure 9 shows the behavior of voltage and current during the energy extraction by means of the converter that feeds the load of the branch. With constant power loads, a decrease in the voltage cause an increase in the current, which cause a further decrease in the voltage. This creates a chain effect: it can be seen how, when the voltage drops under 70% of $V_n$, the current start increasing drastically.

**Influence of the System Components**

The system we used for our model is 1 MW-1000 V. In the model we considered the inductance of the cable, of the output filter, and the capacitance of the output filter.

Successful use of the controlled power sequencing approach depends strongly on features of the system, particularly on the size of the output filter of the main converter and on the characteristics of the dc bus.

The peak amplitude and duration of the fault current depend on the sizes of the output filter capacitor and inductor of the main converter that feeds the dc bus. Analysis shows two main transient events: a first current impulse that depends on the size of the output capacitor and a second slower-decaying current that depends on the size of the output inductor of the converter that feeds the dc bus. Figure 10 illustrates that the behavior of the fault current explored through simulations is similar to those theoretical explained in Figure 1.

Figure 11 shows the equivalent circuit that represents the downstream side of the main converter: $C_{out}$ and $L_{out}$ are the components that are responsible for the two main transient events.
The de-energizing time (current decay and reconfiguration time) depends on characteristics of the dc bus, like the cable impedance and length. Our system model (Figure 1) represents a 1 MW grid operating at 1000 V. We studied several scenarios where the fault occurred at distances from the main converter ranging between 3 and 100 meters. The cable between the main converter and the fault was represented with a \( \pi \) model having the values shown in Table I, in order to consider the cable influence on the de-energizing process.

**TABLE I**

<table>
<thead>
<tr>
<th>( R ) [mOhm/m]</th>
<th>( L ) [( \mu )H/m]</th>
<th>( C ) [nF/m]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.193</td>
<td>0.3051</td>
<td>0.55</td>
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</table>

Ultimately, the behavior of the fault current depends on the characteristics of the filter on the main converter, on the distance of the fault from the main converter, and on the fault impedance. In our model, the main converter has the following characteristics (Table II).

**TABLE II**

<table>
<thead>
<tr>
<th>Switching Frequency [Hz]</th>
<th>L [( \mu )H]</th>
<th>C [( \mu )F]</th>
</tr>
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<tbody>
<tr>
<td>25000</td>
<td>340</td>
<td>280</td>
</tr>
</tbody>
</table>

For a benchmark converter having nominal parameters as shown in Table II, our simulations show that the time to isolate the faulted line is 1.5 ms, with a peak current of 3 kA. This is much faster than a dc circuit breaker [12] can act, and faster even than an AC system where interruption and reconfiguration typically require one to two half-cycles of the ac waveform, or 8-16 ms. Moreover, a load hold-up capacitor of 470 \( \mu \)F allows a 50 kW constant power load on a healthy branch to ride-through with a maximum voltage drop of 30%.

For converters not having the nominal parameters, the protection system parameters must be appropriately adapted. For example, a larger filter capacitance can be compensated by increasing the switching frequency of the main converter. If system components are able to carry current bigger than 3 kA, a larger capacitance for the output filter can be used. Where fault currents can exceed 3 kA, IGBTs are inadequate [13] and mechanical contactors or hybrid contactors [14] must be used instead.

The opening time of contactors is an important part of the reconfiguration process, so speed is of the essence. Choosing hybrid contactors as a solution for our system, we can observe that the time \( t_1 \) to de-energize and to reconfigure the dc bus becomes:

\[
t_1 = t_{de} + t_{cont}
\]

Where \( t_{de} \) is the de-energizing time and \( t_{cont} \) is the time that the contactor or hybrid contactor needs to open faulted circuit. While commercial dc contactors for this kind of system need between 12 ms and 20 ms to open a circuit, a hybrid contactor has an opening time of 0.6 ms. If the contactors on each branch of the bus are sized for the nominal current \( I_n \) of the system, the best performances of the protection scheme are achievable.

The output capacitor of the main converter is one of the most critical components of the system: the time that the fault current takes to decrease to its nominal value depends on the amount of energy accumulated in the output capacitor, which is proportional to its size.

The relationship between the size of output capacitor and the peak fault current can be described with the following empirical expressions (observation range between 5 and 10000 \( \mu \)F):

\[
\frac{I}{C} = \alpha \cdot C^{-0.67}
\]

With \( \alpha \) depending on the distance of the fault from the main converter (Table III):

**TABLE III**

<table>
<thead>
<tr>
<th>Distance [m]</th>
<th>3</th>
<th>30</th>
<th>100</th>
</tr>
</thead>
<tbody>
<tr>
<td>Alpha</td>
<td>2</td>
<td>0.808</td>
<td>0.655</td>
</tr>
</tbody>
</table>
Figure 12 shows the relationship between the size of the output filter capacitor and the peak current duration, and that there is a parallel relationship between the duration of this peak and the size of the capacitor.

The overload capability of the main converter allows the dc bus to draw more than the nominal rated power. This allows the capacitor or other storage elements to be recharged more quickly than they are discharged. Since the energy used to supply loads is equal to the energy the main converter has to replace after reconfiguration (ignoring losses), the recharge of capacitor can be faster that their discharge only if the recharge power is bigger than the nominal one, as shown in (3).

\[ t_{\text{charge}} = \frac{I_n}{I_{\text{MAX}}} \cdot t_{\text{discharge}} \]  

Where \( I_n \) is the nominal current and \( I_{\text{MAX}} \) is the overload current allowed by the main converter. The discharging time corresponds to the time that loads need to be supplied by hold-up capacitors. Thus, the charging time (\( t_{\text{charge}} \)) depends on the discharging time (\( t_2 \)):

\[ t_2 = t_{\text{hold-up}} = t_1 + t_{\text{charge}} \]  

\[ t_2 = \frac{t_d + t_{\text{cont}}}{1 - \frac{I_n}{I_{\text{MAX}}}} \]  

Equation (5) explains how the process time is related to the de-energizing time and the overload capability.

Figure 13 shows how the time to isolate the faulted line (\( t_1 \)) and the entire process time (\( t_2 \)) depend on the size of the output capacitor of the main converter, for several values of output capacitor (100–6000 \( \mu \)F). There is a parallel relationship between the de-energizing time and the fault distance.

The impedance of fault due to a short circuit or a ground fault influences both the fault current and the duration of the protection process. For most of simulations, we adopt as a fault impedance an equivalent resistance of the short circuit fault:

\[ R_f = 0.02 \Omega \]

The variation of the fault impedance influences slightly the performance of the protection process, as shown in Figure 15 for a bus length of 100 meters.
Finally, the ride-through capability for loads on unfaulted branches depends on the entire process time ($t_2$), and on the size of the local hold-up capacitance. The following expression provides a design guideline for the hold-up capacitance:

$$C_{hold-up} = \frac{2 \cdot P_{load} \cdot t_2}{V_n^2 \cdot 0.7}$$

Where $V_n$ is the nominal voltage of the dc bus and $P_{load}$ is the power request of the load of the relative branch. The 0.7 coefficient indicates that the minimum allowed voltage of the capacitor is 70%, which correspond to 50% of the energy accumulated in the capacitor. As presented before (Figure 9), after that point the current increases too fast, making the energy transfer inefficient.

We have shown how system parameters influence the protection scheme performances, and which range of value of parameters leads to the minimum intervention time. Figure 16 shows a comparison among the times required for fault elimination by using the controlled power sequencing, by simply controlling the main converter, and by utilizing traditional circuit breakers.

**CONCLUSION**

We show that a power sequence control scheme can be used to protect a dc power distribution system from line and ground faults. For a typical industrial dc bus, this method is able to eliminate the fault in typically 1.5 ms, whereas for an AC system it is typically 8-16 ms.

We show how the de-energizing and reconfiguration times depend on the output capacitance of the main converter, on the distance to the fault, on the fault impedance, and on the intervention time of the contactors we use to isolate the faulted branches.

Moreover, we explain how to size each hold-up capacitor so as to permit loads on unfaulted circuits to ride through the process uninterrupted.

Our results provide essential guidelines for design of fault protection for dc power systems using power sequencing and they illustrate how to achieve specified reaction times of the protection scheme.

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