The Use of a Formal Optimisation Procedure in Automatic Parameter Extraction of Power Semiconductor Devices

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***Abstract*— A procedure for automatic parameter extraction is outlined, based on accurate physics-based models of the diode, IGBT and associated circuitry. A formal optimisation method is used to refine initial parameter estimates, and is coupled with a hardware testing system to obtain device waveform measurements.**[1]

I. Introduction

One of the primary reasons for device and circuit simulation in power electronic system design is estimation of power losses. The significant source of such losses is generally the switching devices. Hence an accurate and physically-based model is required, as the simulations must be valid over a wide range of conditions. This is also the case in determining other characteristics such as electromagnetic compatibility.

Crucially, the parameters must be found for a good fit with the devices and circuit. Although the use of a physics-based model requires minimal parameter extraction, some refinement of the parameters must take place in order to improve the accuracy of the simulations, given the range of conditions. An automated parameter extraction procedure is essential.

Previous attempts at such a parameterisation procedure have concentrated on either fitting DC characteristics [1] or key performance indicators, for example reverse recovery currents and times in the case of the power diode [2], [3]. None allow a model to be fitted sufficiently to produce accurate power loss estimates.

This paper describes parameter extraction and refinement using a formal optimisation procedure. It is based on accurate device and circuit models coupled with an optimisation algorithm and hardware data acquisition. All of these run from or within MATLAB.

II. Parameterisation Overview

The parameter extraction process can be summarised in the following list and in fig. 1:

1) Initial estimates of parameters made from device datasheets and basic measurements.
2) Measurement of device switching behaviour, i.e. acquisition of switching waveforms.
3) Simulation of circuit behaviour using parameters estimated.

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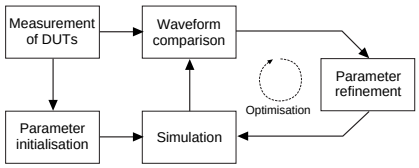

Fig. 1. Diagram showing the procedure of parameter extraction.

4) Comparison of simulated and measured waveforms to produce an error value.
5) Variation of the parameter values to minimise the error value.

Step 5 is the optimisation procedure. Once the error value has been determined, the parameters are varied, and the simulation in step 3 re-executed to produce a waveform valid for that set of parameters. This is again compared to the measured waveform in step 4, and the optimisation continues accordingly. Once the parameters have converged to give a minimum error, the optimisation procedure stops.

Imposing multiple circuit operating conditions should ideally be carried out to ensure that the parameters are valid across a wide operating region.

III. Device and Circuit Models

Most power electronic circuits can be reduced to the standard chopper cell for device simulation purposes, where the voltage across an inductive load is switched at high frequency to produce a particular load current. The cell comprises a switching device, in this case an IGBT, and a freewheel diode to provide a path for the current when the switch is off. Fig. 2 shows the chopper in detail, including lumped stray inductances and the IGBT gate drive. The small junction capacitances of the anti-parallel 'off' devices are represented as a small R-C snubber.

The stray inductance is crucial to the circuit performance. It determines the rate at which the current commutates between the diode and the IGBT when the latter switches on or off. Most importantly, the removal of charge from the diode when it switches off is significantly affected by this inductance, which in turn influences the power dissipation of both devices during this switching event. It can also determine whether the devices approach their maximum ratings during the switching process.

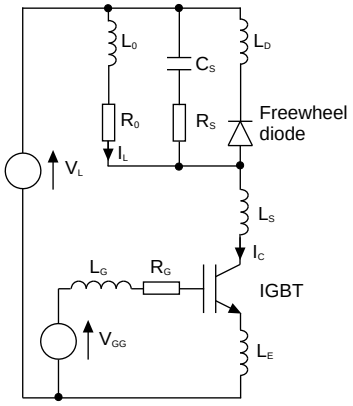

Fig. 2. Single chopper cell (I_L: load current, L_0, R_0: load, L_S, L_D: IGBT and diode stray inductance, L_E: kelvin emitter inductance, L_G: gate inductance, R_G: gate resistance, C_S: Snubber capacitance, R_S: Snubber resistance)

Carrier storage within the lightly-doped base region of a power semiconductor device is critical to the transient response of the device and its behaviour within a particular circuit. IGBTs and diodes both exhibit carrier storage, which enables them to have low on-state voltages at high currents and a high breakdown voltage capability when off.

For diodes, the carrier distribution across the wide drift region is approximately one-dimensional. For IGBTs, it is one-dimensional across 90% of the drift region [4], and so may be reasonably assumed as such for the whole region provided some modifications are made. For both devices, space-charge neutrality is maintained when the device is on, where the majority carrier profile closely matches the minority (injected) carrier profile. Under these conditions, assuming high-level injection, carrier dynamics are described by the classic ambipolar diffusion equation (ADE):

$$D\frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{\tau} + \frac{\partial p(x,t)}{\partial t} \tag{1}$$

Leturcq et al proposed a simple solution of this [5], [6], where the carrier distribution with space at any point in time is transformed into a cosine Fourier series. This effectively reduces a PDE into a set of coupled first-order ODEs. The carrier distribution is therefore given by:

$$p(x,t) = p_0(t) + \sum_{k=1}^{\infty} p_k(t)\cos\left(\frac{\pi k\,(x-x_1)}{x_2-x_1}\right) \tag{2}$$

This requires the boundaries of the undepleted carrier storage region, given by x_1 and x_2, and the carrier gradients at these points, see fig. 3. The latter are derived from the corresponding hole and electron currents at the boundaries.

The advantage of using such a model is that the physicality is retained. It is a geometrically-based model, and includes no ill-defined parameters. Thus little refinement is required after a first estimate of the parameters, since the model should be valid across a wide range of conditions.

The models of the devices and circuit are implemented within the MATLAB/Simulink environment. MATLAB is a general-purpose mathematical computation package used

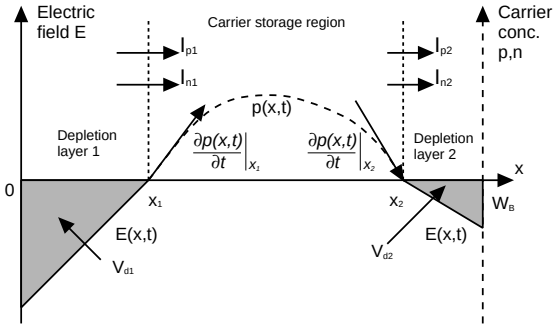

Fig. 3. Arrangement of the carrier storage region and depletion layers within the distributed Fourier model.

widely throughout mathematics, science and engineering. Simulink is a graphical front-end, primarily intended for simulation of dynamic systems in classic block-diagram form. These have been used successfully both to model and optimise the interaction of the IGBT, diode and circuit [7].

Implementation of the device models requires setting up the relevant physical processes in block diagram form for graphical entry into Simulink. The model uses the hierarchical visualisation offered by Simulink to simplify its development and appearance.

IV. Parameter Initialisation

The initial parameter estimation is based on datasheet values and simple measurements. The procedure has been described in previous literature [8], [9] and will only be summarised here, see table I.

V. Hardware Setup

The circuit is based on a full-bridge converter, see fig. 4. The devices under test are arranged as a half-bridge, which will simply act as a chopper if the load current I_0 is unidirectional, and the other leg behaves as an active load to set the current. The supply voltage V_{DC} may be set using a third leg as a boost converter.

TABLE I
Device parameters and estimation.

Diode	Area, A	Forward DC current, I_F
		Maximum current density, J
	Lifetime, τ	Forward DC current, I_F
		Reverse recovery charge, Q_{RR}
	Base width, W_B	Breakdown voltage, V_{BD}
		Ionisation coefficients, a, b
	Base doping, N_B	Est. 1×10^{14}
IGBT	Area, A	Forward DC current, I_F
		Maximum current density, J
	Intercell ratio, a_i	Capacitances C_{rss}, C_{oss}
	Base doping, N_B	Variation of capacitances
		C_{rss}, C_{oss} with voltage
	Lifetime, τ	Tail current, I_T
	Base width, W_B	Breakdown voltage, V_{BD}
	Recombination parameter, h_p	Tail current threshold
	MOS transconductance, K_p	Datasheet I-V plots
	Gate capacitance, C_{GE}	Datasheet gate charge
	Oxide capacitance, C_{OX}	Datasheet gate charge
	Threshold voltage, V_{th}	Datasheet
	Gate length, l_m	Capacitance C_{rss}

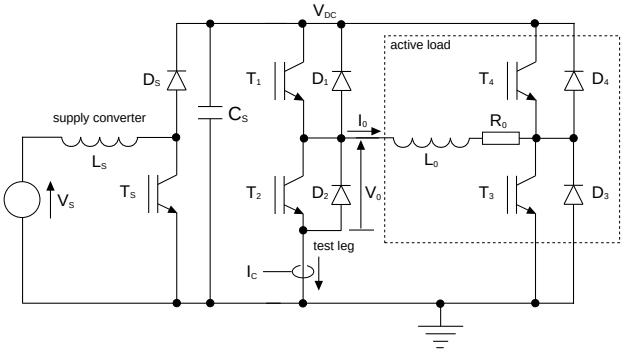

Fig. 4. Circuit used in hardware setup.

The conditions are set using a controller implemented in a field programmable gate array (FPGA) which generates the required PWM gate drive signals from the conditions supplied by the host PC. The acquisition of the waveforms is carried out using a LeCroy Waverunner LT344L digital oscilloscope connected to the host PC. This allows transfer to data files which the parameter extraction procedure, running in MATLAB, can access to extract the waveforms.

Here, the circuit is operated in steady-state mode with a DC load current. This is set to be negative, so that the lower IGBT T_2 and the upper diode D_1 are the active devices. The measured waveforms are:

- V_{GG} The output voltage of the gate drive.
- V_{GE} The gate-emitter voltage at the lower IGBT, using the kelvin emitter connection.
- V_{CE} The voltage at the leg output, relative to the negative DC link rail.
- I_C The current returning from the leg to the negative DC link rail.

The device under test is a Toshiba IGBT module, MG75J6ES50, rated at 600V, 75A. The DC link voltage V_{DC} is set to 200V and the load current I_0 to two values: 11A and 20A. The duty ratio is 0.5, and the switching frequency is 25kHz, giving a period of 40μs. Each acquired waveform has a duration of 50μs, giving a margin of 5μs either side of the complete switching cycle. At a sample rate of 200MHz this gives 10^4 samples per waveform.

VI. Waveform Evaluation

One possible method of comparison of the measured and simulated waveforms is using the salient points of the waveforms, e.g. diode reverse recovery current, reverse recovery time or IGBT switching time. This gives a small number of points to match, but suffers from low accuracy. Most importantly, the waveforms may differ quite substantially during the switching instants, especially in di/dt and dv/dt. This would give a large error in estimated power during simulation.

A much more accurate method of comparison is to simply calculate the sum of the squared errors at each time point in the waveforms. However this requires:

- A method to compare the different traces of each waveform, typically voltage and current.
- Normalisation of the errors used, so that the conditions imposed such as supply voltage and load current do not affect the consistency of the parameter extraction.
- Accurate synchronisation of the waveforms, otherwise the errors in di/dt and dv/dt will be significant and lead to inaccuracy of the power loss estimates during simulation.

Since accurate power loss estimation is the goal of the parameter extraction, it is sensible to use instantaneous power loss as the basis for the error. It also encompasses the most critical points in matching the voltage and current traces, since maximum instantaneous power dissipation is usually where di/dt and dv/dt are high. Normalisation should be performed before the power dissipation is calculated.

Summing the squared errors, rather than the magnitudes of the errors, assigns more significance to any large errors between measured and simulated waveforms. This is useful since it forces the optimisation to reduce the large errors first and converges quickly.

Typically, synchronisation is carried out 'by eye', and matches both the time scales and the slopes (di/dt and dv/dt). A simple synchronisation is to align the gate drive signals, which are available in both the hardware and the simulation used and are square waves [4]. An alternative is to compare the instantaneous power dissipations and find the relative delay of the waveforms which produces the minimum error between them. This removes the effect of the gate drive circuit, which may be useful in diode parameterisation. However estimation of the gate drive parameters is essential in IGBT parameterisation, as these are critical to IGBT operation. In this case the simple synchronisation is appropriate.

In either case, synchronising manually is not appropriate here where many simulations are performed. Instead, the cross-correlation between the traces is calculated.

The cross-correlation between two continuous signals can be defined as:

$$r_{xy}(\tau) = \int_{-\infty}^{+\infty} x(t+\tau)\, y^*(t) dt \tag{3}$$

For discrete signals, which is the case here since the waveforms are sampled, the cross-correlation is:

$$r_{xy}[k] = \sum_{n=-\infty}^{+\infty} x(n+k)\, y^*(n) \tag{4}$$

If the waveforms are similar enough, which will be the case since the model is relatively accurate and the initial parameter set should give reasonable results, then the time delay τ or k at which the cross-correlation is at a maximum equals that which will produce the best matching. The appropriate function in MATLAB is `xcorr`, which in this case is set to produce the unbiased estimate of the correlation:

$$c_{xy,unbiased}(k) = \frac{1}{N-k} \sum_{n=0}^{N-k-1} x(n+k)\, y^*(n) \tag{5}$$

The correlation of the gate waveforms uses a window of length 2μs either side of the gate step. Once the matching

delay is determined, the error between the waveforms can be calculated at each point, squared and summed to produce a single error estimate. The windows used for the error estimation are set to 90% of the on- or off-state period.

A summary of the waveform evaluation process is:

1) Align the waveforms by finding the maximum correlation of the gate drive references.
2) Normalise and window the waveforms and calculate the instantaneous power dissipations.
3) Sum the squares of the errors across the period of comparison.

VII. Parameter Optimisation

Optimisation techniques rely on finding the minimum of an *objective function*. This is specific to a particular problem, and must be a function of the system parameters. The optimum set of parameter values will give the minimum objective function, which is in this case the error between the measured and simulated waveforms.

Common optimisation techniques used in power engineering, including the design of circuits, components and machines, are optimisation by steepest descent, simulated annealing and genetic algorithms. Steepest descent, a traditional method of optimisation, suffers from only being able to find a local minimum, not necessarily the global minimum, and is dependent on the start position. This can be ameliorated using additional heuristics such as a variant of the Tabu Search [10]. Simulated annealing and genetic algorithms find the global minimum more effectively by introducing random parameter variation [11]. The advantage of using these is their complete and relatively quick search of the parameter space. However this is only of benefit where the objective function is likely to be multi-modal, and thus contain many minima.

In the case of parameterisation the starting point is likely to lead directly to the global minimum since the model is accurate and the initial parameter set should be a good estimate. Hence a simple direct search, without additional heuristics, may be used. In addition, the search time must be kept reasonably low, particularly since the number of parameters is high, giving a large parameter space. Using genetic algorithms or simulated annealing would increase the search time prohibitively.

In the direct search [12], locating a minimum relies on the method of steepest descent. For analytic objective functions, the gradient can be calculated at any point. Frequently though, the objective function is not an analytic function of the parameters, and as this is the case here, the use of the direct search is dictated. Therefore the objective function must be evaluated at points surrounding the current position in the parameter space.

The Hooke and Jeeves Search [13] is a variant on the direct search. After evaluating the objective function at points surrounding the current (base) point, a move in a particular direction is made, and then a test is made to see if further movement in the same direction would give another reduction in the objective function. This is known as a *pattern move*, and can increase the speed at which the minimum is reached. It is particularly useful with a large number of parameters, where the cost of re-evaluating the space surrounding a particular point is high. A feature from the Tabu Search is added, which ensures that points visited recently (i.e. the last M base points) are not re-visited. M is typically between 5 and 10 for small-scale problems (up to 12 parameters), and is set to 8 here. Finally, when the minimum has been found the average parameter set of the 6 best points is calculated and evaluated to see if this results in an improvement. If not, the search terminates. Figure 5 shows a graphical example of the direct search with two variables.

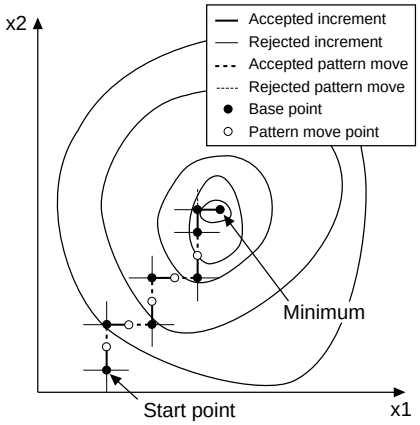

Fig. 5. Example of Hooke & Jeeves direct search with two variables.

VIII. Results

The waveforms acquired from the oscilloscope and used for parameterisation with I_0 = 11A can be seen in fig. 6. The timebase is 5μs per division.

The devices parameters were then estimated using the methods mentioned in section IV. The parameters chosen for optimisation, and the trends in parameter values during optimisation, can be seen in table II. Note that some parameters reached the limits imposed to avoid excessive parameter variation, marked by an asterisk (*). SSE refers to the sum of the squared errors between the measured and simulated waveforms for each set of parameters.

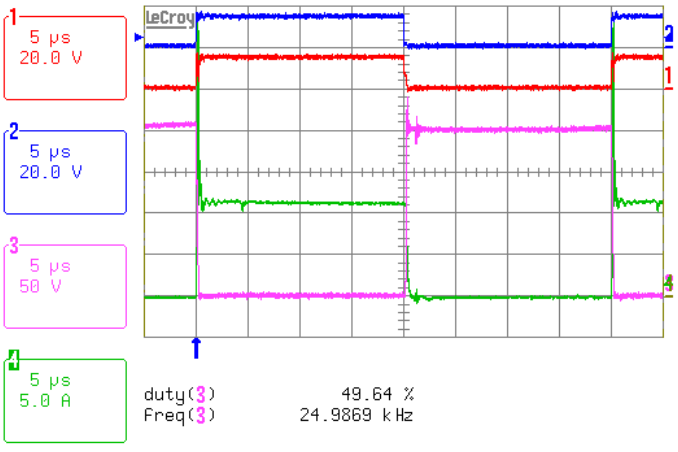

Fig. 6. Device waveforms used in parameterisation
Traces: 1: V_{GE}, 2: V_{GG}, 3: V_{CE}, 4: I_C

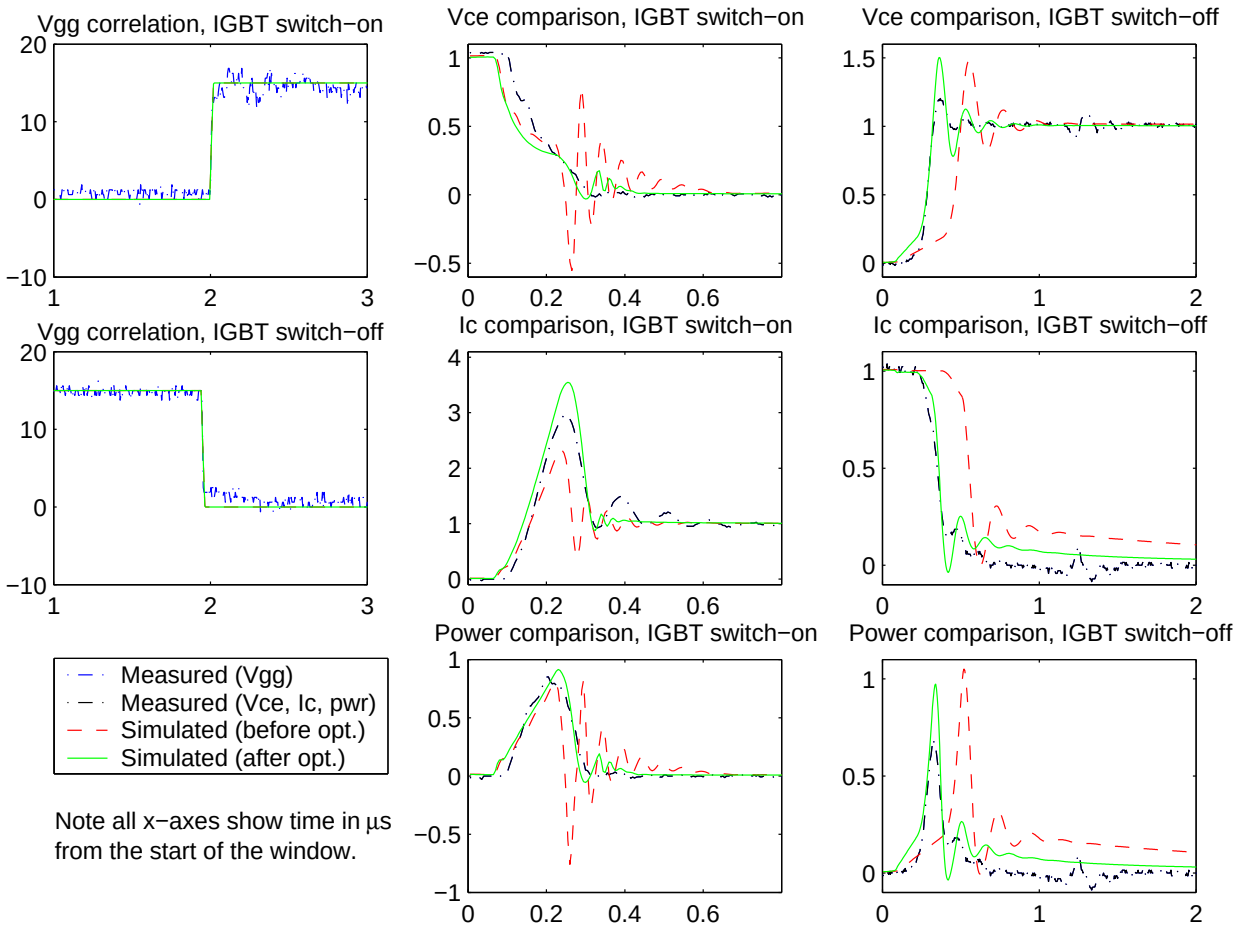

Fig. 7. Waveforms taken from the correlation and error estimation windows (I_0 = 11A)

Fig. 7 shows the waveforms before and after optimisation, compared to those acquired from the oscilloscope. I_0 is 11A here. In all waveforms the x-axis gives the time in μs from the start of the window.

The left-hand waveforms show the measured and simulated V_{GG} waveforms, after synchronisation, and are in volts. The V_{CE} and I_C waveforms refer to the leg output voltage (referred to the bottom connection of the leg) and the current through the lower half of the leg respectively. These are normalised to the off-state voltage (200V) and on-state current (11A), and are then multiplied to give the power waveforms.

TABLE II

DEVICE PARAMETERS BEFORE AND AFTER OPTIMISATION

	Param.	Before	After 11A	After 20A	Units
Diode	A	1.0	1.5*	1.5*	cm^2
	W_B	150	101	80*	μm
	N_B	1e14	2e14	4e14	cm^{-3}
	τ	0.15	0.378	0.18	μs
IGBT	A	1.0	1.0	1.0	cm^2
	W_B	150	100*	100*	μm
	N_B	3.3e14	3.3e14	3.3e14	cm^{-3}
	τ	63.5	100*	100*	μs
	h_p	2e-12	1e-11*	1e-11*	$cm^4 s^{-1}$
	a_i	0.25	0.25	0.25	-
	l_m	6.0	6.0	6.0	μm
	C_{OX}	20	10	10	$nFcm^{-2}$
Circuit	L_D	600	487	522	nH
	L_S	150	50*	50*	nH
SSE	-	38.0	6.4	5.7	-

IX. DISCUSSION

The parameter trends during optimisation are similar for both load conditions. The same parameters remained constant for both conditions. The trends in those which varied are the same, and any differences present are generally small, indicating that the models retain physicality and are independent of conditions.

The waveforms in fig. 7 show a clear improvement in simulation accuracy over the course of the optimisation. At turn-on, the large oscillations in V_{CE} are reduced, although the current overshoot increases. The optimisation has not captured the gentle oscillation in current after the overshoot, as this does not contribute greatly to the power dissipation. The large oscillations present before optimisation clearly give significant errors in the power dissipation.

At turn-off, the delay in switching is the primary cause of the error. Synchronising using V_{GG} is demanding but appears appropriate. The V_{CE} waveforms show that the delay before optimisation is rectified by a reduction in plateau duration, corresponding to the initial slow rise in voltage. In addition, the tail current I_C is reduced in height, despite an increase

in IGBT lifetime, and is due to the substantial increase in IGBT emitter recombination (h_p increases by a factor of five). This is a consequence of using a non-punch-through (NPT) IGBT model and limiting the base width W_B. Allowing W_B to reduce further and using a punch-through (PT) model may improve the tail current matching.

To match the power dissipation, the optimisation can inadvertently increase the current and decrease the voltage (or vice-versa), giving incorrect voltage and current waveforms but reasonably accurate power losses. Evidence of this can be seen at turn-on, where the under-estimate of voltage has been compensated for by an increase in current overshoot, resulting from an increase in diode lifetime. This is one example of how the optimisation process can allow deficient features of one device, or indeed the circuit, to be compensated by incorrect parameter variation elsewhere. Hence the models become more behavioural and less physical. This may be acceptable for a single operating condition, but as the conditions will generally vary in actual circuit operation this will lead to inaccurate simulation results. While using instantaneous power only has limitations, it gives reasonable di/dt, dv/dt, voltage, current and power matching, and this is what one requires in a design.

The possibility of behavioural models being inadvertently created could be reduced by separating the optimisation of the diode and IGBT. However this will depend on having accurate parameter estimates for the device *not* being fitted. This suggests that the diode and IGBT should initially be treated as a unit and parameters extracted accordingly. This agrees with observations made previously regarding the coupling between their behaviour [7]. Later device-specific optimisation can then be undertaken to reduce the effects of the rest of the circuit. The merits of separate and simultaneous parameter extraction should be investigated more thoroughly.

In addition, the optimisation may try to compensate for inaccuracies in the models if these are significant enough. Here, the stray inductances and capacitances in the circuit due to the module interconnections and anti-parallel 'off' devices have not been fully accounted for, and any further work should include a thorough investigation of these. Also, scope for improving the accuracy of the device models is limited because of the need to keep the simulation time low. This is necessary because the large number of parameters, each of which must be varied at every point in the optimisation, requires a very large number of simulation runs.

The disadvantage of basing the objective function on the sum of the squared errors (SSE) is that it will focus more on matching the switching losses than the on-state losses. This is because the instantaneous on-state losses are much smaller in magnitude, and become smaller still when squared. Using the magnitudes of the errors rather than the squares may help to redress this imbalance.

Finally, it should be noted that the parameterisation in its current form has only attempted to match the measurements and simulation at a few operating points. Ideally, it should be swept through the whole range of expected conditions in order to give a more reliable estimate of the parameters, and hence more accurate simulation under varying conditions. This will require continuous acquisition of data during the optimisation, which is feasible since MATLAB can control both the hardware (via RS-232) and the oscilloscope (via ethernet and ActiveX). Modification of the optimisation procedure to allow for multiple conditions would also have to be undertaken.

X. Conclusions

The concepts introduced provide a solid foundation for automated parameter extraction. The use of MATLAB as a common environment allows simple implementation of the extraction procedure. The optimisation results show a clear improvement in simulation accuracy from the initial parameter estimates.

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