Parameter Extraction Procedure for Vertical SiC Power JFET

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Abstract — A practical parameter extraction procedure for power silicon carbide (SiC) junction field effect transistor (JFET) is presented. The carrier mobility and carrier concentration are very important parameters, strongly affecting the device current capability and dynamic characteristics for a given design. When modeling JFETs, values of these parameters are usually based on assumptions and given by a vendor in a range. As a result, model accuracy is compromised. In this paper, a step-by-step parameter extraction procedure is described that includes extraction of mobility and carrier concentration in the channel and drift regions based on knowledge of device geometrical parameters. For the first time, carrier mobility in channel and drift regions of power JFET are extracted individually. It is found that channel and drift region mobilities can be very different for a given device, since they are strongly fabrication-process dependent. Separate extraction of these two mobilities will also improve model accuracy in case of imperfect knowledge of device geometry. The developed procedure includes extraction of empirical parameters describing the temperature dependency of mobilities in the channel and drift regions. A simple static I-V characterization and C-V measurements are the only measurements required for the parameter extraction. 1

Index Terms—JFET switches, Power semiconductor devices, Silicon carbide JFETs, parameter extraction.

I. INTRODUCTION

Silicon carbide (SiC) is one of the most promising semiconductor materials for next-generation power semiconductor switching devices. Currently, significant improvements in SiC material and device fabrication have been made, so that high-power SiC devices such as MOSFETs and JFETs are expected to appear on the market in the near future. Since SiC high power devices are still under development, there is a need to create accurate and validated models for SiC prototype devices to allow power converter designers to predict the impact of the new devices on system performance and facilitate device commercialization. To make a model practical, it is very important to provide the extraction procedure for the parameters employed in the model description. While comprehensive techniques for MOSFET parameter extraction have been developed, very limited work has been done for high power JFET. This can be explained by the fact that silicon (Si) JFETs are used for very low power applications and power Si JFET appeared on the market for only a short time, before being replaced by the more advantageous Si MOSFET. The goal of this paper is the development of a simple parameter extraction procedure for power JFET, which can be used in conjunction with any physics-based JFET model.

Generally, SiC device electrical models use an empirical expression for carrier mobility such as (1) [1],[2], despite the fact that it is well known that this parameter may vary over quite a wide range, depending on processing parameters such as temperature, annealing conditions, defect density, stoichiometry, and so on [3]-[5].

\[
\mu(T) = \frac{947}{1 + \left( \frac{N_D}{1.94 \times 10^{17}} \right)^{0.67} \left( \frac{T}{300} \right)^{2.15}}
\]  

(1)

In a power JFET both channel and drift region give significant contribution to the device on-resistance and consequently to forward voltage drop during forward operation. Therefore, it is important to consider these regions as two individual regions with different electrical properties. Firstly, carrier concentration in the drift region is typically an order of magnitude lower than that in the channel region, which consequently results in higher carrier mobility in drift region. Secondly, carrier mobility in the drift region can vary in quite a wide range depending on growth method [3] (sublimation or chemical vapor deposition (CVD)) and doping process used to achieve semi-insulation property of the blocking layer. There are basically two techniques to fabricate semi-insulating SiC material: high-purity semi-insulating (HPSI) process, where low unintentional doping is obtained by means of purification of gasses, growth chamber etc.; and vanadium-doped semi-insulating (VDSI) process, where unwanted donor doping is compensated by introduction of vanadium atoms. It was demonstrated that carrier mobility of HPSI material can be twice as high as that of VDSI material, 113 cm²/V-s vs 66.9 cm²/V-s respectively [4]. It was shown in [5] that C/Si ratio during CVD growth of semi-insulating SiC significantly affects the trap density and controlling this parameter makes it possible growing an
ultrahigh purity SiC material with carrier mobility of 981 cm²/V-s.

From a device modeling standpoint, carrier mobility is the most important parameter determining the current capability of the device for a given design. Small changes in mobility significantly affect device characteristics and, for accurate prediction of the electrical behavior, this parameter has to be known precisely. In this paper, for the first time, carrier mobilities in channel and drift region of power JFET are extracted individually. This is important, because the two mobilities can be significantly different depending on fabrication, as explained above. Another advantage of the proposed procedure is that carrier concentrations in the channel and in the drift region are also considered as technological parameters and are explicitly extracted. These carrier concentrations, as the mobilities discussed above, have a significant effect on device behavior and are not precisely known. The uncertainty comes again from fabrication, and also from incomplete dopant ionization at ambient temperature – the so-called carrier freezing in SiC.

JFET operation is briefly reviewed in Section II, the proposed parameter extraction procedure is described in Section III and experimentally validated in Section IV.

II. BRIEF REVIEW OF JFET OPERATION

A compact physics-based model for vertical power SiC JFET with the structure shown in Fig. 1 was recently developed and validated [6]. In this section device operation is described with reference to this model, in order to identify required physics-based parameters to be extracted. However, the device parameters obtained from this extraction procedure could be used with a different physics-based JFET model. Please note that the procedure as described applies to the vertical JFET structure of Fig. 1. Modifications of this extraction procedure to apply it to lateral-channel JFETs [7] are possible but are outside the scope of this paper.

The modeling is applied to an equivalent single-cell structure as shown in Fig. 1. An actual power JFET is a large area device and it is usually realized as a grid of individual cells connected in parallel by top metallization. For simplicity of model description, the real structure is replaced by a single cell with a length $Z$ (perpendicular to the page) equal to the sum of lengths of all individual grid cells. There is no structural difference between a normally-on and a normally-off JFET. This property of JFET is determined by the width of the channel region and its doping concentration only. Depending on application goal these two parameters can be designed in such a way, so that channel is fully depleted (normally-off) or partially depleted (normally-on) under zero gate bias condition.

Output characteristics of the JFET exhibit two distinct operating regions: the linear region in which channel current is approximately proportional to channel voltage, and the saturation region in which channel current is approximately constant. In the linear region, corresponding to small drain-source voltage, the depleted region of the channel is determined by gate voltage and it has an approximately uniform width along the channel. Equation (2) describes the JFET electrical behavior in the linear region:

$$I_{CH} = I_P \times \left\{ \frac{3V_{CH}}{V_P} - \frac{2}{V_P^{\frac{1}{2}}} \times \left( (V'_{CH}-V_{GS}+V_{bi})^{\frac{1}{2}} -(V_{bi}-V_{GS})^{\frac{1}{2}} \right) \right\}$$

(2)

In this equation $I_{CH}$ is the channel current, which is equal to the JFET drain current, $V_{CH}$ is the channel voltage, $V_{GS}$ is the gate-source voltage, $V_{bi}$ is the built-in voltage, $I_P$ is the pinch-off current and $V_P$ is the pinch-off voltage.

With further increase of channel voltage, the depletion region becomes progressively wider towards the drain side (see Fig. 1) causing a reduction of channel width and an increase of channel resistance. As a result, JFET current saturates. Another possible reason for current saturation is carrier velocity saturation due to the presence of high electric field in the channel. In the saturation region electrical behavior of the device is described by:

$$I_{CH\text{SAT}} = I_P \times \left\{ 1 - 3 \frac{V_{bi}-V_{GS}}{V_P} + 2 \left( \frac{V_{bi}-V_{GS}}{V_P} \right)^{\frac{1}{2}} \right\} \times \left[ 1 + \lambda (V_{CH}-V_{CH\text{SAT}}) \right]$$

(3)
Pinch-off current $I_p$ and pinch-off voltage $V_p$ are defined as:

$$I_p = \frac{Z \cdot \mu_0 \cdot q^2 \cdot N_{CH}^2 \cdot a^3}{3\varepsilon_{SC} \cdot L_{eff}}$$

(4)

$$V_p = \frac{q \cdot N_{CH} \cdot a^2}{2 \cdot \varepsilon_{SC}}$$

(5)

An empirical constant parameter $\lambda$, called the channel-length modulation coefficient, determines the increase of current in saturation region in equation (3). Extraction of this parameter from the slope of saturated I-V characteristics is described in any electronics textbook and therefore is not discussed in this paper. The boundary between linear and saturation region is given by the saturation voltage $V_{CHSAT}$, which is the channel voltage at which the JFET enters the saturation region. This voltage is a linear function of applied gate voltage and is given by (6).

$$V_{CHSAT} = V_p + V_{GS} - V_{bi}$$

(6)

The voltage $V_{CH}$ is the effective voltage applied to the channel and it is equal to the drain-source voltage reduced by the drift region voltage drop:

$$V_{CH} = V_{DS} - I_{CH}R_{DRIFT}$$

(7)

where drift region resistance is given by:

$$R_{DRIFT} = \frac{L_{DRIFT}}{q \cdot \mu_{DRIFT} \cdot N_{DRIFT} \cdot Z \cdot W_{DRIFT}}$$

(8)

From equations (3), (4), and (5) it can be concluded that one of the most important parameters which establishes current level in the saturation regime is the channel half-width $a$, which appears cubed in (4) and squared in (5). The on-resistance of the JFET in the linear region is determined mostly by carrier mobilities in the channel and drift regions. In order to predict the device behavior in the full range of the operational conditions it is necessary to establish temperature dependencies of mobility in the channel and drift regions. These mobilities can be described by empirical equations similar to (1). As part of the proposed parameter extraction procedure, extraction of parameters describing the temperature dependence of mobilities will be discussed.

Table I shows the complete list of JFET parameters and the technique used for extraction. The first four geometrical parameters are assumed to be known for the proposed parameter extraction procedure. A fifth geometrical parameter, the drift region length $L_{DRIFT}$, may be assumed to be known, or can be extracted from breakdown voltage measurements.

<table>
<thead>
<tr>
<th>JFET Parameter</th>
<th>Extracted From</th>
</tr>
</thead>
<tbody>
<tr>
<td>$a$ : Half width of channel region</td>
<td>Geometrical parameters assumed to be known</td>
</tr>
<tr>
<td>$L$ : Channel length</td>
<td>Breakdown voltage measurement</td>
</tr>
<tr>
<td>$Z$ : Equivalent single-cell device thickness</td>
<td>Threshold voltage measurement or capacitance measurement</td>
</tr>
<tr>
<td>$W_{DRIFT}$ : Width of drift region</td>
<td>Linear region of forward characteristics</td>
</tr>
<tr>
<td>$N_{DRIFT}$ : Majority carrier density in drift region</td>
<td>Carrier mobility at different temperatures</td>
</tr>
<tr>
<td>$L_{DRIFT}$ : Length of drift region</td>
<td>Saturation region of forward characteristics</td>
</tr>
<tr>
<td>$V_p$ : Pinch-off voltage</td>
<td>Carrier mobility at different temperatures</td>
</tr>
<tr>
<td>$N_{CH}$ : Majority carrier density in channel region</td>
<td></td>
</tr>
<tr>
<td>$\mu_{CH}(T)$: Carrier mobility in channel region</td>
<td></td>
</tr>
<tr>
<td>$\mu_{DRIFT}(T)$: Carrier mobility in drift region</td>
<td></td>
</tr>
<tr>
<td>$x$: Carrier mobility temperature dependence parameter</td>
<td></td>
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<tr>
<td>$\lambda$ : Channel modulation effect coefficient</td>
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</table>

### III. Parameter Extraction Procedure

The parameter extraction approach discussed in this paper is based on the assumption that device geometrical parameters $a$, $L$, $Z$, $W_{DRIFT}$ are known. Channel-length modulation coefficient $\lambda$ is extracted from the slope of I-V characteristics in the saturation region [8].

**A. Drift Region Parameters $N_{DRIFT}$, $L_{DRIFT}$**

C-V measurements can be performed to extract drift region carrier concentration $N_{DRIFT}$. The measurement setup is shown in Fig. 2a.
A negative gate bias is needed for a normally-on device to provide complete depletion of the channel. For a normally-off device this condition is already satisfied with zero gate bias by internal device design. When channel is fully off, depletion region is located entirely inside drift region and the depletion boundary cross-section, which represents the area of the equivalent capacitor, corresponds to the known effective area of the device. Therefore, capacitance between gate and drain can be represented by a capacitor having plates with an area \( A = Z \cdot W_{\text{DRIFT}} \) (see Fig. 1) and spacing between them equal to the depleted width of the drift region \( W_D \).

\[
C_{GD} = \frac{\varepsilon_{SC} Z \cdot W_{\text{DRIFT}}}{W_D} \tag{9}
\]

On the other hand, to deplete a thickness \( W_D \) of semiconductor material having carrier concentration \( N_{\text{DRIFT}} \), the required voltage \( V_{DS} \) is given by:

\[
W_D = \sqrt{\frac{2 \varepsilon_{SC} (V_{DS} + V_b)}{q N_{\text{DRIFT}} \varepsilon}} \tag{10}
\]

Substituting equation (10) into equation (9), an expression for carrier concentration as a function of applied voltage and corresponding capacitance can be obtained:

\[
N_{\text{DRIFT}} = \frac{2(V_{DS} + V_b) C_{GD}^2}{q \varepsilon_{SC} Z^2 W_{\text{DRIFT}}^2} \tag{11}
\]

Note that equation (11) is valid only under the assumption that the drift region is uniformly doped. In case of nonuniform dopant distribution in the drift region, its profile along the drift region can be estimated by (see [9] for details):

\[
N_{\text{DRIFT}}(W_D) = \frac{2}{q \varepsilon_{SC} Z^2 W_{\text{DRIFT}}^2} \frac{d(1/C_{GD}^2)}{dV_{DS}} \tag{12}
\]

Keithley CV analyzer 590 was used to perform measurements in this work. Output voltage of the analyzer was applied to the drain of the tested JFET and the input of the analyzer was connected to the gate of the device to measure displacement current of gate-drain capacitance as shown in Fig. 2a. Progressively increasing drain bias voltage during the measurement, capacitance is measured by superimposing a small AC voltage component. From (11) one can see that, if drift region carrier concentration is constant, the quantity \( 1/C_{GD}^2 \) varies linearly with drain-source voltage \( V_{DS} \). From the plot in the inset of Fig. 2b two distinct slopes can be identified. This indicates that for studied JFET the drift region contains two distinctive regions.
with different doping concentration. At a depth of approximately 1.4μm from the channel edge carrier concentration in drift region reaches its lowest value and remains constant. There are two possible reasons for nonuniform carrier distribution in the drift region. First, there may be a transition layer intentionally formed between drift and channel regions to reduce stress introduced by materials with different concentrations of dopant. Second, depletion edge surface may not be flat when it approaches the channel region, thus changing the effective area of the plates of studied capacitance $C_{GD}$. Higher values of $V_{DS}$ give more accurate results because the edge of the depletion region is absolutely flat, while it starts to be deformed when approaching the channel region. Knowing the capacitance at a given drain-source voltage, the depletion width, introduced by this voltage, is calculated using (10), and then carrier distribution along the drift region is calculated using (12). The result is shown in Fig. 2c for the region corresponding to drain-source voltages between 20V and 40V, which correspond to a region far into the drift region.

Nondestructive breakdown voltage measurements can be performed to evaluate drift region length $L_{DRIFT}$. Slowly increasing drain-source reverse bias and carefully monitoring the sudden increase in leakage current, breakdown voltage for a given structure is estimated. To optimize high power device in both the forward and the reverse regime of operation, the drift region design is a trade-off between high blocking capability and low on-resistance. The punched-through structure is commonly used to improve this trade-off, because the desired blocking voltage can be obtained with a smaller drift region thickness, with associated smaller on-state resistive drop. Assuming punched-through design, the drift region thickness $L_{DRIFT}$ can be obtained by solving the breakdown voltage equation [8]:

$$V_{PT} = \frac{E_{\text{crit}}}{2} \left( 2L_{\text{Drift}} - \frac{L_{\text{Drift}}^2}{W_{\text{dep}}} \right)$$  \hspace{1cm} (13)$$

where $W_{\text{dep}}$ is the depletion width for non-punched-through design

$$W_{\text{dep}} = \frac{\varepsilon_{\text{SiC}}}{qN_{\text{Drift}}} E_{\text{crit}}$$ \hspace{1cm} (14)$$

**B. Channel Carrier Concentration $N_{CH}$**

In order to extract the carrier concentration in the channel, one can proceed as follows: first, extract the threshold voltage $V_{TH}$ either from the device transfer characteristics or from a $C_{GS} - C_{GD}$ measurement, then use this value to calculate the pinch-off voltage $V_P$, finally use equation (5) to calculate the channel carrier concentration from the calculated $V_P$.

The threshold voltage $V_{TH}$ is extracted from transfer characteristics of the device as shown in Fig. 3a (for details about threshold voltage extraction see [10]). Alternatively, the threshold voltage can be extracted using a capacitance measurement technique, evaluating the change of $C_{GS}$ and $C_{GD}$ as a function of applied gate-source voltage. When voltage increases, $C_{GD}$ gradually increases due to reduction of depleted portion of drift region. At the moment when the gate voltage corresponds to the threshold value, the channel opens and $C_{GD}$ abruptly drops down due to reduction of effective area of plates of $C_{GD}$ capacitance. At the same time capacitance $C_{GS}$ abruptly increases due to channel opening. Note that when gate-source voltage is below the threshold value, $C_{GS}$ remains almost constant because of the fully depleted channel region.

Threshold voltage can be considered the value of gate-source voltage for which the saturation voltage is zero (the forward characteristic for $V_{GS} = V_{TH}$ has no linear region and saturates at zero drain-source voltage). Therefore, substituting $V_{GS} = V_{TH}$ and $V_{CH\text{SAT}} = 0$ in (6), the pinch-off voltage is given by (15).

$$V_P = V_{hi} - V_{TH}$$ \hspace{1cm} (15)$$

Only two parameters, the width of the channel region and its doping concentration, determine the pinch-off voltage of a device. The pinch-off voltage for both normally-on and normally-off devices can be evaluated from (15), where $V_{TH}$ is threshold voltage or external voltage applied to the gate in order to open the channel for conduction. The difference between normally-on and normally-off devices is that, for a normally-off JFET, built-in voltage $V_{bi}$ of gate-source junction is sufficient to fully deplete the channel and threshold voltage is positive, while, for a normally-on device, built-in voltage $V_{bi}$ only partially depletes the channel and threshold voltage is negative, because an additional reverse bias is needed to fully deplete the channel. Pinch-off voltage is positive for both structures Using (5), carrier concentration in the channel is calculated as:

$$N_{CH} = \frac{2 V_P \varepsilon_{\text{SiC}}}{q a^2}$$ \hspace{1cm} (16)$$
The carrier mobility can be extracted from the linear region of the output characteristics of the JFET, assuming that channel and drift layer can be represented as two rectangular-shaped regions of constant cross-section. Neglecting contact resistance, the on-resistance of JFET can be represented as the sum of channel and drift region resistances.

\[ R_{\text{ON}} = R_{\text{CH}} + R_{\text{DRIFT}} \]

\[ = \frac{L}{2q\mu_{\text{CH}} N_{\text{CH}} Z(a-W_s)} + \frac{L_{\text{DRIFT}}}{q\mu_{\text{DRIFT}} \cdot Z \cdot W_{\text{DRIFT}}} \]  

(17)

where \( W_s \) is

\[ W_s = \sqrt{\frac{2\varepsilon_e (V_{th} - V_{GS})}{qN_{CH}}} \]  

(18)

The lowest on-resistance occurs when the channel is completely open for current transport \((V_{GS} = 3V \text{ for 4H-SiC normally-off device})\), and drain voltage is small \((V_{GS} \gg V_{DS})\), which ensures that channel cross-section is uniform along the entire channel length. The drift region of a power JFET is made relatively thick to support high blocking voltage, so that it can be assumed that effective drift region cross-section does not change significantly under low \( V_{DS} \). In other words, current spreading effects where the channel meets the drift region can be neglected. Thus, the difference in initial \((V_{DS} \approx 0)\) on-resistance of two curves in the family of static characteristics of the device is determined only by change of channel resistance, while drift region resistance is a constant for any gate voltage. The carrier mobility in the channel can be extracted using two I-V curves corresponding to different gate bias as shown in Fig. 4. The inverse of the slope around the origin of a forward characteristic gives the on-state resistance for given gate bias. Two such resistances \( R_{\text{ON1}} \) and \( R_{\text{ON2}} \) are shown in Fig. 4. Using expression (17) for the two resistances and subtracting the expressions so obtained, the drift resistance cancels out and, after rearranging, one obtains the desired expression for mobility:

\[ \mu_{\text{CH}} = \frac{L(W_{S1} - W_{S2})}{2qN_{CH} Z(R_{\text{ON1}} - R_{\text{ON2}})(a-W_{S1})(a-W_{S2})} \]  

(19)

Note that this derivation neglects the reduction of drift region thickness and extension of channel into drift region. Carrier mobility in the drift region can then be calculated using the I-V curve corresponding to fully open channel:

\[ \mu_{\text{DRIFT}} = \frac{L_{\text{DRIFT}}}{q N_{\text{DRIFT}} \cdot Z \cdot W_{\text{DRIFT}} \left( R_{\text{ON2}} - \frac{L}{2q\mu_{\text{CH}} N_{\text{CH}} Z(a-W_{S1})} \right)} \]  

(20)

The accuracy of the model extraction depends strongly on an accurate knowledge of the channel geometry. The extracted values of mobilities in drift and channel regions can deviate from real material characteristics, but proposed parameter extraction procedure successfully accomplishes the main goal of matching an experimental static family of curves with simulated characteristic in the linear region of operation.
Fig. 4 Output characteristics of normally-off SiC JFET

In order to predict the device behavior in the full range of operational conditions, the present parameter extraction procedure can be extended with the goal to establish temperature dependencies of mobility in the channel and drift regions. The proposed model for temperature dependant mobility takes the form of empirical expression (1). The first term in equation (1) represents the carrier mobility in the region with given carrier concentration \( N_D \) at 300K temperature. Therefore, equation (1) can be rewritten as:

\[
\mu(T) = \mu_{300} \left( \frac{T}{300} \right)^{x}
\]  

(21)

where \( \mu_{300} \) is the mobility in the given region (channel or drift) extracted at room temperature using the above described procedure based on experimental data. Extrapolation parameter \( x \) is calculated using values of the mobilities extracted from static characteristics at room temperature and at an elevated temperature \( T_1 \):

\[
x = \frac{\ln \left( \frac{\mu(T_1)}{\mu_{300}} \right)}{\ln \left( \frac{T_1}{300} \right)}
\]  

(22)

Figure 5 shows a comparison of mobilities in drift and channel regions obtained from experimental static characteristics and mobilities predicted using (21) and (22).

Fig. 5 Extracted and simulated mobilities of JFET

IV. EXAMPLE OF PROCEDURE IMPLEMENTATION

The parameter extraction procedure is applied to a normally-off JFET sample provided by SemiSouth. After all JFET parameters are extracted (see Table II), they can be plugged into the model described in Section II for validation. Fig. 6 shows simulated (solid lines) output characteristics of SiC JFET based on parameters extracted from experimental (dots) static characteristics measured at room temperature and 100ºC. The simulated I-V curves are in very good agreement with experimental characteristics in linear region, which validates the proposed mobility extraction procedure. The matching of the modeled and experimental characteristics in the saturation region is a matter of model adjustment, considering field dependence of mobility and some uncertainty in geometrical parameters. The model was particularly sensitive to the value of channel half width \( a \). The parameter extraction approach proposed in this work can accompany practically any physics-based JFET model, while the equations for mobility extraction (17), (19) and (20) may need to be modified depending on device geometrical considerations.
<table>
<thead>
<tr>
<th>JFET Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$a$ : Half width of channel region</td>
<td>Known from manufacturer</td>
</tr>
<tr>
<td>$L$ : Channel length</td>
<td></td>
</tr>
<tr>
<td>$Z$ : Equivalent single-cell device thickness</td>
<td></td>
</tr>
<tr>
<td>$W_{DRIFT}$ : Width of drift region</td>
<td></td>
</tr>
<tr>
<td>$N_{DRIFT}$ : Majority carrier density in drift region</td>
<td>7x10$^{15}$ cm$^{-3}$ from C-V characteristic Fig. 2c, equation (12)</td>
</tr>
<tr>
<td>$L_{DRIFT}$ : Length of drift region</td>
<td>10.2 $\mu$m from equations (13) and (14)</td>
</tr>
<tr>
<td>$V_P$ : Pinch-off voltage</td>
<td>2.5 V using equation (15)</td>
</tr>
<tr>
<td>$N_{CH}$ : Majority carrier density in channel region</td>
<td>3x10$^{15}$ cm$^{-3}$ using equation (16), with $V_{TH}$ extracted from Fig. 3a</td>
</tr>
<tr>
<td>$\mu_{CH}(T)$ : Carrier mobility in channel region</td>
<td>$\mu_{CH} = 171.8 \left( \frac{T}{300} \right)^{-2.5}$ from characteristics in Fig. 6 using equation (19)</td>
</tr>
<tr>
<td>$\mu_{DRIFT}(T)$ : Carrier mobility in drift region</td>
<td>$\mu_{Drift} = 279.6 \left( \frac{T}{300} \right)^{-1.28}$ from characteristics in Fig. 6 using equations (19) and (20)</td>
</tr>
<tr>
<td>$x$: Carrier mobility temperature dependence parameter</td>
<td>-2.2 and -1.28 for channel and drift regions respectively</td>
</tr>
<tr>
<td>$\lambda$ : Channel modulation effect coefficient</td>
<td>0.0247</td>
</tr>
</tbody>
</table>

### V. CONCLUSION

The proposed parameter extraction approach allows obtaining major material properties of JFET: carrier concentrations and carrier mobility in channel and drift regions. The developed procedure includes extraction of parameters used in a proposed empirical temperature dependant mobility model. Separate extraction for channel and drift region mobility models is proposed. Validity of the approach is verified by comparison of experimental and simulated results at room temperature and 100ºC. The simulated I-V curves are in very good agreement with experimental characteristics in the linear region thanks to the separately extracted drift region and channel region mobilities.
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