A Resonant Drive Circuit for GaN Power MOSHFET

Background of the Research
The research on wide-band III-Nitride semiconductor materials such as GaN is rapidly developing. These materials have some unique properties, including high electron mobility and saturation velocity, high sheet carrier concentration at heterojunction interfaces, high breakdown voltages, low thermal impedance (when grown over SiC or bulk AlN substrates), chemical inertness, and radiation hardness [1]. These properties make III-Nitride technology a promising approach for high-power, high-temperature applications. When applied to power electronics, the AlGaN/GaN Heterostructure Field-Effect Transistors (HFETs) allow for high-power switching with sub-microsecond and nano-second switching times. Insulated-gate III-Nitride HFETs (MOSHFETs) allow to further increase the achievable power levels and improve the high-temperature stability. Currently, however, drivers for GaN-MOSHFET switches are not available in the market. Some driver circuits for power Si-MOSFETs can be modified to drive the MOSHFET switches, but the highest frequency at which they can work is less than five MHz. The purpose of this work is to design a new generation of drivers for III-Nitride MOSHFETs that can best exploit the operation speed of those devices.

Challenges of the Design
Though desirable, making the switch work at high frequencies cannot be easily done. The switch operation speed is limited primarily by its efficiency. When a switch works at high switching frequencies, its switching power loss surges rapidly, and accordingly the overall efficiency declines. Another challenge is that the MOSHFET is a Zero-Voltage-Switch-ON switch: that means it needs a zero voltage to turn on and negative voltage to turn off. This control characteristic is the same of IGBTs and opposite of that p or n channel MOSFET the power devices usually used in power electronics.

Introduction of the Reference Resonant Drive Circuit
Many research projects devoted to gate high frequency switches are reported in the literature [2][3][4][5][6][8]. The more suitable approach to cope with the high efficiency requirement is resonant gate-driving technique. The switching loss reduction critical in high frequency application is obtained by means of resonant transitions in a ad hoc L-C circuits that involves the gate-drain parasitic capacitance of the MOSHFETs [7]. Figure 1 and Figure 2 show the circuit and waveforms for this reference circuit [7].

In conventional MOSFET drivers, the switching power loss are \( P_{\text{loss}} = Q_{\text{DD}} \times V_{\text{DD}} \times f_s = C_{\text{iss}} \times V_{\text{DD}}^2 \times f_s \).

By means an L-C resonant circuit topology and two clamp diodes, the power losses are reduced to:

\[
P_{\text{loss}} \approx \frac{R_G}{(R_G + Z_0)} \times Q_{\text{DD}} \times V_{\text{DD}} \times f_s = \frac{R_G}{(R_G + Z_0)} \times C_{\text{iss}} \times V_{\text{DD}}^2 \times f_s \tag{1}
\]

where:

- \( R_G \) is the equivalent gate resistance: the parasitic gate resistor of the power MOSFET switch, the on resistances of the drive transistors and the parasitic resistance of the inductor, etc are included;
- \( C_{\text{iss}} \) is the parasitic input capacitance of the power transistor \( M_1 \);
Clearly, the smaller the MOSFET gate resistance is, the smaller the power loss will be [7]. Unfortunately, this solution is not directly applicable to MOSHFET devices due to their particular control characteristic: a negative gate-source voltage is required to turn off the devices and a level shifter must be provided.

**Introduction of the New Drive Circuit for GaN MOSHFET**

This paper will present a new resonant drive circuit specifically designed for III-N MOSHFETs. This topology based upon the resonant gate drive circuits described above, solve the problems underlined. The schematic of the circuits is shown in Figure 3 and in the Figure 4 are reported relevant waveforms in the approximation of ideal switches.

The operation of the circuit is described as follows. Let’s consider the operation begins at the negative storage position when $V_{gs_{-MOSHFET}}$ is equal to $V_{p-}$ and both $M_P$ and $M_N$ are turn off. At time 0, when $M_P$ turns on, inductor current $i_{LR}$ begins to flow and charges the parasitic capacitor $C_{iss}$ of the MOSHFET switch. When the voltage across the $C_{iss}$ reaches the value slightly higher than zero at $t_1$, the diode D1 conducts and clamps $V_{gs_{-MOSHFET}}$ at zero, and the inductor current continues to flow freewheeling along D1. At time $t_2$, when $M_P$ turns off, the inductor current decreases, which makes the diode D3 conduct, and the inductor current flows through the path VSS-D3-$L_R$-D1-GND and returns energy back to the voltage source. Between $t_2$ and $t_3$, the inductor current $i_{LR}$ decreases from $I_p$ to zero and the gate-source voltage of the switch remains at zero. At time $t_4$, transistor $M_N$ turns on, and the inductor current begins to flow in the opposite direction, discharging the MOSHFET parasitic capacitor $C_{iss}$, until the voltage across $C_{iss}$ reaches the maximum value $V_{p-}$ at $t_5$.

At the same time, the diode D2 prevents the opposite resonant inductor current from flowing and the voltage $V_{gs_{-MOSHFET}}$ remains at $V_{p-}$ until the transistor $M_P$ turns on at $t_6$; then the same process repeats. In equation (2), the effect of the diode is neglected since Schottky diodes are used and the forward voltage is very small compared to the source voltage. This assumption applies to all the following discussions in the paper.

**Advantages of the New Resonant Driver for GaN MOSHFET Switches**

An analytical estimation of the power losses has been conducted and it is worth pointed out the main advantages offered by the topology described:

(1) LC resonant tank and a totem-pole driving pair are inherited from the reference driver to reduce the power loss. In the traditional driver circuit, an inductor is used to act with the parasitic capacitor of the GaN switch as a resonant tank. The inductor current and the power losses of the circuit are described by the following equations making reference to the same symbols used in (1):

$$
Z_0 = \sqrt{\frac{L_R}{C_{iss}}}, \quad f_s \quad \text{is the switching frequency}
$$
\[ I_{LR}(t) = \frac{R_G}{2L_R} e^{- \frac{4L_R}{C_{iss}} t} \sqrt{\frac{R_G}{2L_R}} \sin \left( \frac{4L_R R_G e^2}{2L_R} t \right) \]  

\[ P_{loss} \approx \frac{R_G}{(R_G + Z_o)} \cdot P_{conserve} \]  

The equation (4), confirms the linear dependence of the power loss on the parasitic resistance of the GaN. The energy necessary for the commutation flows through the auxiliary drive’s MOSFET and diodes, the LC tank and the gate resistance. Because the LC tank can recover part of the energy and the losses in the auxiliary are little the dissipated power can be limited. For GaN-based MOSFET switches, the parasitic capacitor is small, and only a small inductor is required allowing a driver size reduction.

(2) The circuit has a resonant voltage clamp switch on transition: diode D1 is used to clamp the voltage to zero. Diodes D1 and D3 act together to provide a low impedance path for the inductor current and return the drive energy back to the voltage source after the turn on transient. In Figure 4, when M_P is turned on by a negative pulse, the inductor current begins to flow and the capacitor voltage starts to rise, until at time t1, when the current reaches the peak value \( I_p = V_{ss} + \frac{1}{2} \) and the gate-source voltage of the GaN switch equals zero, the diode D1 conducts and clamps the gate-source voltage to zero. Then, when the input signal comes back to zero, M_P turns off and the inductor current flows through D1 and D3 and returns energy back to the voltage source.

(3) This circuit simplifies the role of the shifter circuit and reduces the overall power loss. As reported in Figure 4 and Equation (2), when M_N turns on, a negative inductor current begins to discharge the gate-source capacitor, and if the gate parasitic resistance of the GaN switch is small, the gate-source voltage starts to decrease and it can reach a higher level negative peak value \( V_{p-} \). The power consumed in this circuit is:

\[ P_{conserve} = Q_G \cdot V_{pp} \cdot f_s = C_{iss} \cdot V_{pp} \cdot V_{ss} \cdot f_s = C_{iss} \cdot V_{pp} \cdot V_{ss} \cdot f \]  

where \( V_{pp} \) is the peak-peak voltage across the capacitor \( C_{iss} \).

Combining Equation (4) and Equation (5), the power loss in this drive circuit is described by the following equation:

\[ P_{loss} \approx \frac{R_G}{(R_G + Z_o)} \cdot P_{conserve} = \frac{R_G}{(R_G + Z_o)} \cdot C_{iss} \cdot V_{pp} \cdot V_{ss} \cdot f_s \]  

The turn off transient is not regulated by voltage clamp diodes so the absolute value of \( V_{p-} \) is greater than the absolute value of \( V_{ss} \). A small voltage source can be used to generate a higher gate-source voltage for the switch, and this function will lower the demand for a level shifter circuit and reduce the power loss of the circuit at the same time.

(4) Diodes D1 and D2 make this circuit high tolerance for timing variation. Small pulse widths variation of the control signal does not effect the switching process. The inductor current freewheeling time only is increased, and it does not affect the discharging process since diode D2 prevents the opposite inductor current from flowing. This function lowers the requirement for accurate pulse-width control signals.

(5) The inverter changes the polarity of the input control signals. If the threshold voltage required to turn off the GaN MOSFET switch is much higher than \( V_{p-} \) (\( V_{p-} < V_{gs\_MOSFET} \)), level shifter circuits are required to change the voltage level of the input control signals.

(6) Using ASIC technology to implement part of the circuit increases the operating frequency. Today, since high voltage PMOS and NMOS operate well on 0.8um process, the part of the circuit in the dotted block in Figure 3 can be integrated into an ASIC instead of using discrete components, and this integration will further increase the operation frequency of the driver and simultaneously reduce the size of the circuit.
Decreasing the parasite resistance of the GaN MOSHFET switch reduces the power loss. The GaN MOSHFET switch discussed in this paper is designed and fabricated at USC, and much progress is still being made to improve the characteristics of these devices; an example of such an improvement is a small parasitic gate resistance to reduce the power loss.

Simulation Results
A 40MHz driver has been designed, according to the circuit schematic shown in Figure 3, for drive the GaN MOSHFET switches, produced in the USC microelectronic laboratory. Low resistance and high frequency transistor pair have been choused for the supplementary drive (ZXMD63P02X and ZXMD63N02X) and Schotty diodes (10bq015) for the recovery path.

A full set of Aim-Spice simulation has been completed using relevant models for all the components. A complete characterization of the GaN MOSHFET has been carried out.

In Figure 5 the simulation result for 25MHz switching frequency with pulse width of 7.5ns for the input control signals are reported. The rise time $t_r$ is about 3ns, and the fall time $t_f$ is about 4ns.

Future Work
A prototype board realization for the drive circuit proposed is in progress at Microelectronic Laboratory of University of South Carolina. in the final paper with experimental test

The final paper will include experimental results and measurements for the proposed driver implementation. Further improvements in the circuit operation using ASIC technology will be considered.

REFERENCES


