An Efficient High-Frequency Drive Circuit for GaN Power HFETs

Bo Wang, *Member, IEEE,* Naveen Tipirneni, *Member, IEEE,* Marco Riva, *Member, IEEE,* Antonello Monti, *Senior Member, IEEE,* Grigory Simin, *Senior Member, IEEE,* and Enrico Santi, *Senior Member, IEEE*

***Abstract*—The requirements for driving gallium nitride (GaN) heterostructure field-effect transistors (HFETs) and the design of a resonant drive circuit for GaN power HFET switches are discussed in this paper. The use of wideband III-nitride (such as GaN) devices today is limited to telecom and low-power applications. The current lack of high-frequency high-power drivers prevents their application in power converters. The proposed circuit is based upon resonant switching transition techniques, by means of an LC tag, to recover part of the power back into the voltage source in order to reduce the power loss. This circuit also uses level shifters to generate the zero and negative gate–source voltages required to turn the GaN HFET on and off, and it is highly tolerant to input-signal timing variances. The circuit reduces the overall power consumed in the driver and thus reduces the power loss. This is particularly important for high-frequency driver operation to take full advantage, in terms of efficiency, of the superior switching speed of GaN devices. In this paper, the topology of the low-power-loss high-speed drive circuit is introduced. Some simulation results and preliminary experimental measurements are discussed.**

***Index Terms*—Gallium nitride (GaN) heterostructure field-effect transistors (HFETs), high speed, resonant drive circuit.**

I. Introduction

THE RESEARCH on wideband III-nitride semiconductor materials (such as GaN) has been rapidly developing in the past few years. These materials have unique properties, including high electron mobility, high saturation velocity, high sheet-carrier concentration at heterojunction interfaces, high breakdown voltages, low thermal impedance (when grown over SiC or bulk AlN substrates), chemical inertness, and radiation hardness [1]. Compared with Si FETs, GaN heterostructure field-effect transistors (HFETs) have lower specific on-resistance due to the high-density 2-D electron gas (i.e., above 10^{13} cm^{-2}) and high electron mobility (i.e., above 1500 cm^2/V). As shown in Fig. 1, the static on-resistance of GaN HFETs is almost three orders lower than that of Si MOSFETs, reaching as low as 3.4 m$\Omega \cdot$ cm^2 as introduced in [2].

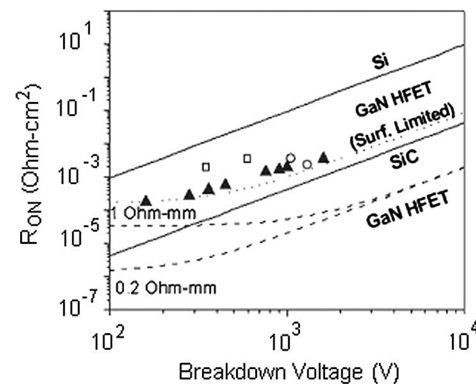

Fig. 1. On-resistance comparison of HFET and SiC transistors.

GaN HFETs can work at high temperature ranges which Si MOSFETs cannot reach, and they also have higher breakdown fields than Si MOSFETs due to the large bandgap energy of GaN material. The III-nitride transistors have been shown to operate at up to 300 °C [3], with no noticeable parameter degradation, and can have high breakdown voltages (up to 1600 V) [2]. Furthermore, the switching speeds of GaN HFETs are expected to be higher than those of Si MOSFETs due to the small input capacitance (for example, the input capacitance for a 100-V 1-A GaN HFET device is about 2 pF, while it is 150–200 pF for a 100-V 1-A power MOSFET). Both the low input capacitor and the low on-resistance are important to obtain good switching characteristics. When applied to power electronics, the AlGaN/GaN HFETs allow for high-power switching with submicrosecond and nanosecond switching times. These properties make the use of III-nitride technology a promising approach for high-power, high-temperature, high-speed, and high-efficiency applications. Using insulated-gate III-nitride HFETs (MOSHFETs) further increases the achievable power levels and improves high-temperature stability.

The described characteristics would be extremely useful in industrial power-electronic application and would improve the efficiency and the regulation in ac–dc and dc–dc converters.

Paper IPCSD-08-056, presented at the 2006 Industry Applications Society Annual Meeting, Tampa, FL, October 8–12, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Power Electronics Devices and Components Committee of the IEEE Industry Applications Society. Manuscript submitted for review November 1, 2007 and released for publication July 9, 2008. Current version published March 18, 2009. This work was supported by the U.S. Office of Naval Research under Grant N00014-05-1-0734 and Grant N00014-07-1-0603.

B. Wang, G. Simin, and E. Santi are with the Department of Electrical Engineering, University of South Carolina, Columbia, SC 29208 USA (e-mail: wangb@engr.sc.edu; simin@engr.sc.edu; santi@engr.sc.edu).

N. Tipirneni is with the Advanced Technology and High Voltage MOSFET Group, Vishay Siliconix, Santa Clara, CA 95054 USA (e-mail: tipirneni.naveen@gmail.com).

M. Riva is with the Department of Physics, Università degli Studi di Milan, 20133 Milan, Italy (e-mail: riva@unimi.it).

A. Monti is with the Institute for Automation of Complex Power Systems, E.ON Energy Research Center, RWTH Aachen University, 52056 Aachen, Germany (e-mail: amonti@eonerc.rwth-aachen.de).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIA.2009.2013578

0093-9994/$25.00 © 2009 IEEE

Authorized licensed use limited to: University of South Carolina. Downloaded on February 15,2010 at 14:40:21 EST from IEEE Xplore. Restrictions apply.

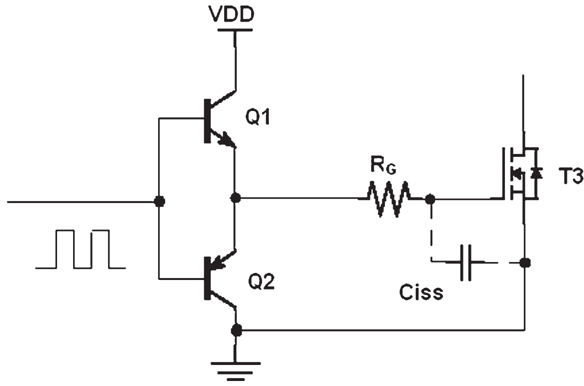

Fig. 2. Complementary emitter follower driver topology.

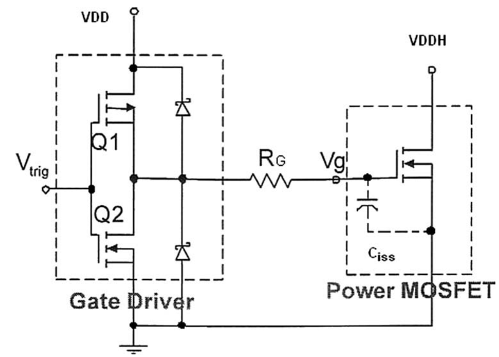

Fig. 3. "Totem-pole" driver schematic.

However, drivers for GaN HFET switches are not currently commercially available. This is one of the factors preventing their application to power converters [4]. Modified driver ICs for power Si-MOSFETs can be used to drive the HFET switches; unfortunately, most of them work at low frequencies (below 1 MHz) [5]–[8]. A few of the driver ICs can work at around 5 MHz; however, the output impedance characteristics of these drivers are not compatible with the GaN devices and can lead to unnecessary power loss [9]–[11]. The purpose of this paper is to design a driver for III-nitride HFETs, which can best exploit the characteristics of these devices and make available their use in power electronic circuits.

II. Considerations for the Design

GaN HFETs have transfer characteristics similar to junction FETs—blocking current when the gate is driven negative and conducting when the gate has zero voltage. Consequently, a negative voltage needs to be generated to turn off the device, and zero voltage is required to turn it on. At the same time, a drive current with a proper value needs to be provided to charge and discharge the input capacitor of the device and support high-frequency operations.

Designing a gate driver that will operate a GaN HFET to its full switching performance presents major technical challenges. When a device works at high switching frequencies, switching power loss starts to dominate the losses, resulting in a decline of the overall efficiency of the circuit. In order to make GaN HFETs work at high frequencies, it is critical to design a drive circuit which can reduce the switching power loss of the devices.

III. Introduction of the Reference Drive Circuits

A. Basic Drive Circuit for Si MOSFETs

Typically, the conventional gate-drive circuit is constituted by complementary devices—either a pair of emitter followers in a class B amplifier, as shown in Fig. 2, or pMOS and nMOS in a "totem-pole" configuration, as shown in Fig. 3. These devices supply the charge needed for the input capacitance (C_{iss}) and allow the switch to turn on and off [12], [13]. C_{iss} represents the equivalent input capacitance accounting for the gate–source and Miller capacitances. These approaches offer an easy schematic, well suited for low-frequency applications. However, when the frequency increases, both the losses due to the switching operations in the auxiliary MOSFETs Q_1 and Q_2 and the losses in the gate port of the power MOSFET become unacceptable [13].

In conventional MOSFET drivers, the consumed switching power depends directly on the switching frequency f_{s} and parasitic input parameters [13]

$$P = Q_{\mathrm{DD}} VDD f_{\mathrm{s}} = C_{\mathrm{iss}} VDD^2 f_{\mathrm{s}} \tag{1}$$

where

C_{iss} input capacitance;

Q_{DD} gate charge needed to charge C_{iss} of the power transistor from zero to VDD.

Equation (1) is only correct for low-frequency operations when the cross-conduction loss for the complementary pair is small enough to be neglected. When the operation frequency increases, the cross-conduction loss increases and cannot be neglected.

B. Basic Resonant Drive Circuit

Many techniques have been proposed for driving semiconductor devices at high frequencies of which [12]–[15] were considered to present a scheme, resonant gate driving, which is most suitable for coping with the high-efficiency requirement of HFETs. In this topology, the switching-loss reduction, critical in high-frequency applications, is obtained by means of resonant transitions in an *ad hoc* $L-C$ circuit that involves the input capacitance of the switches.

Fig. 4 shows the schematic for a basic resonant circuit. The principle of the circuit operation is that the energy stored in the capacitor is recycled and then stored back in the capacitor with the opposite polarity voltage. Thus, the energy is always stored in the capacitor; however, the "effective" capacitor voltage is alternated between positive- and negative-voltage states. In this way, a quasi-square-wave voltage can be imposed on the capacitor in a low-loss manner. The process described earlier is achieved when an inductor and a capacitor are resonating together, with resonance being stopped when the capacitor voltage is either at a maximum or minimum [14].

The circuit works under zero voltage and low negative voltage supply (VSS). It generates an output voltage from VSS_High to V_POS (where VSS_High is a high negative

Authorized licensed use limited to: University of South Carolina. Downloaded on February 15,2010 at 14:40:21 EST from IEEE Xplore. Restrictions apply.

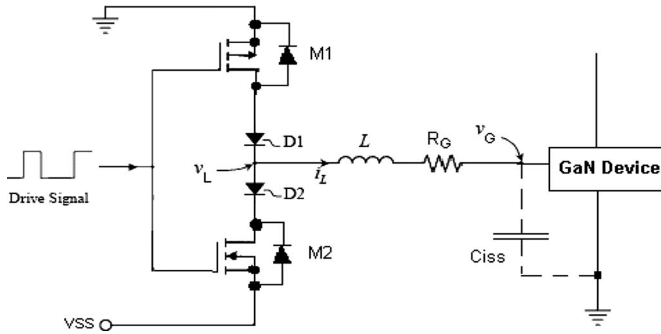

Fig. 4. Basic resonant drive circuit.

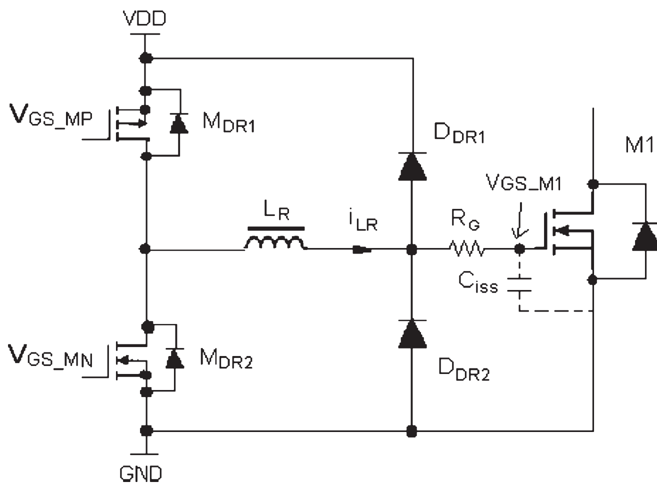

Fig. 5. Resonant driver with efficient energy recovery in [15].

voltage with greater absolute value than VSS and V_POS is a positive voltage). The values of V_POS and VSS_High depend on the Q factor of the resonant circuit and the supply voltage VSS. However, for GaN HFETs applications, one of the key problems is that high forward gate leakage currents cause degradation of device parameters. When the gate voltage becomes positive, the forward leakage current shunts the gate-channel capacitance, limiting both the maximum device current and the reliability of the device [1]. Consequently, avoiding positive gate–source voltage becomes a fundamental requirement, and therefore, the drive circuit shown in Fig. 4 is not suitable for driving GaN HFETs.

C. Resonant Circuit With Efficient Energy Recovery

1) Circuit Introduction: A low-loss high-speed voltage-clamping efficient energy-recovery resonant circuit is introduced in [15]. Figs. 5 and 6 show the resonant circuit and its relevant waveforms, respectively.

The operation of the circuit is described as follows, beginning at the negative storage position when $V_{\rm GS}$ is equal to zero and both $M_{\rm DR1}$ and $M_{\rm DR2}$ are turned off. At time t_1, when pMOS $M_{\rm DR1}$ turns on, the inductor current $i_{\rm LR}$ begins to flow and charges the input capacitor $C_{\rm iss}$ of the MOSFET switch M_1. The resonant is built up through VDD, $M_{\rm DR1}$, the resonant inductor $L_{\rm R}$, and the input capacitor $C_{\rm iss}$. Due to the resonance,

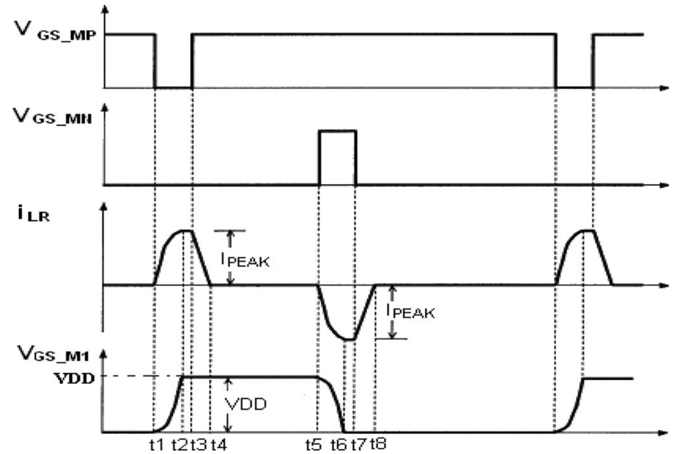

Fig. 6. Waveforms of the resonant driver circuit in [15].

both the voltage $V_{\rm GS}$ and current $i_{\rm LR}$ will increase sinusoidally, with the following resonance period:

$$T = \frac{2\pi}{\omega_0} = 2\pi\sqrt{L_{\rm R}C_{\rm iss}} \quad (2)$$

where ω_0 is the resonance frequency.

When the gate voltage reaches VDD, the inductor current reaches its peak at $I_{\rm peak} = VDD/Z_0$ (where Z_0 is the L–C characteristic impedance $Z_0 = \sqrt{L_{\rm R}/C_{\rm iss}}$. The rise time is $t_{\rm r} = t_2 - t_1 = T/4$.

When the voltage across $C_{\rm iss}$ reaches the value slightly higher than VDD at t_2, the diode $D_{\rm DR1}$ conducts and clamps $V_{\rm GS}$ at VDD, and the inductor current continues to flow, freewheeling along $D_{\rm DR1}$. At time t_3, when $M_{\rm DR1}$ turns off, the inductor current decreases, which makes the body diode of $M_{\rm DR2}$ conduct, resulting in the inductor current flowing from the GND to VDD by way of the body diode of $M_{\rm DR2}$, $L_{\rm R}$, and $D_{\rm DR1}$ and returning energy to the voltage source. Between t_3 and t_4, the inductor current $i_{\rm LR}$ decreases from $I_{\rm PEAK}$ to zero, and the gate–source voltage of the switch remains at VDD.

At time t_5, the nMOS transistor $M_{\rm DR2}$ turns on, and the inductor current begins to flow in the opposite direction, discharging the MOSFET gate capacitor $C_{\rm iss}$. When the gate voltage $V_{\rm GS}$ reaches zero, the inductor current reaches its negative peak current at $-I_{\rm peak} = -VDD/Z_0$, and $t_{\rm r} = t_6 - t_5 = T/4$. Until the voltage across $C_{\rm iss}$ is slightly lower than zero at t_6, the diode $D_{\rm DR2}$ conducts and clamps $V_{\rm GS}$ at zero, and the inductor current continues to flow, freewheeling along $D_{\rm DR2}$. At time t_7, when $M_{\rm DR2}$ turns off, the inductor current increases, which makes the body diode of $M_{\rm DR1}$ conduct, and the inductor current flows from GND to VDD by way of $D_{\rm DR2}$, $L_{\rm R}$, and the body diode of $M_{\rm DR1}$ and returns energy to the voltage source. Between t_7 and t_8, the inductor current $i_{\rm LR}$ increases from $-I_{\rm PEAK}$ to zero, and the gate–source voltage of the switch remains at GND [15].

2) Power-Loss Calculation: There are three types of power loss in the drive circuit: conduction loss, switching loss, and cross-conduction loss. The resonant drive circuit in Fig. 5 can reduce them all.

Conduction loss: From the description reported earlier, it is clear that the conduction loss of the drive circuit can be

Authorized licensed use limited to: University of South Carolina. Downloaded on February 15,2010 at 14:40:21 EST from IEEE Xplore. Restrictions apply.

reduced by using the resonant drive topology to recover part of the gate-drive energy.

Assuming that the initial value of the gate voltage is $V_{\rm GS}$ and the initial value for the inductor current is $I_{\rm LR}$, the inductor current $i_{\rm LR}(t)$ and gate voltage $V_{\rm GS}(t)$ can be calculated by using the following:

$$i_{\rm LR}(t) = C_{\rm iss}\frac{dV_{\rm GS}(t)}{dt} \tag{3}$$

$$V_{\rm GS}(t) = VDD - R_{\rm G}i_{\rm LR} - L_{\rm R}\frac{di_{\rm LR}}{dt}. \tag{4}$$

Solving (3) and (4) obtains

$$\begin{aligned} i_{\rm LR}(t) =& I_{\rm LR}e^{-\frac{R_{\rm G}}{2L_{\rm R}}t}\cos\left(\frac{\sqrt{\frac{4L_{\rm R}}{C_{\rm iss}} - R_{\rm G}^2}}{2L_{\rm R}}t\right) \\ &+ \frac{2VDD - 2V_{\rm GS} - R_{\rm G}I_{\rm LR}}{\sqrt{\frac{4L_{\rm R}}{C_{\rm iss}} - R_{\rm G}^2}} \\ &\cdot e^{-\frac{R_{\rm G}}{2L_{\rm R}}t}\sin\left(\frac{\sqrt{\frac{4L_{\rm R}}{C_{\rm iss}} - R_{\rm G}^2}}{2L_{\rm R}}t\right). \end{aligned} \tag{5}$$

During the charging phase, the initial values are $V_{\rm GS} = V_{\rm GS}(t_1) = 0$ and $I_{\rm LR} = I_{\rm LR}(t_1) = 0$; solving (5) using these two values results in

$$i_{\rm LR}(t) = \frac{2VDD}{\sqrt{\frac{4L_{\rm R}}{C_{\rm iss}} - R_{\rm G}^2}}e^{-\frac{R_{\rm G}}{2L_{\rm R}}t}\sin\left(\frac{\sqrt{\frac{4L_{\rm R}}{C_{\rm iss}} - R_{\rm G}^2}}{2L_{\rm R}}t\right). \tag{6}$$

Assuming that $Z_0 \gg R_{\rm G}$, (6) can be simplified to

$$i_{\rm LR}(t) \approx \frac{VDD}{\sqrt{\frac{L_{\rm R}}{C_{\rm iss}}}}e^{-\frac{R_{\rm G}}{2L_{\rm R}}t}\sin\left(\frac{1}{2}\sqrt{\frac{1}{L_{\rm R}C_{\rm iss}}}t\right). \tag{7}$$

Consequently, the energy dissipation by the series gate resistor $R_{\rm G}$ equals

$$\begin{aligned} E_{\rm charge} &= \int_{t_1}^{t_2} R_{\rm G}i_{\rm LR}^2(t)dt \\ &= \int_0^{t_{\rm r}} R_{\rm G}i_{\rm LR}^2(t)dt \\ &= \frac{\pi VDD^2R_{\rm G}C_{\rm iss}^{3/2}}{4\sqrt{L_{\rm R}}} \\ &= \frac{\pi VDD^2R_{\rm G}C_{\rm iss}}{4Z_0}. \end{aligned} \tag{8}$$

During the discharging phase, $V_{\rm GS} = V_{\rm GS}(t_5) = VDD$, and $I_{\rm LR} = I_{\rm LR}(t_5) = 0$. Using these values to solve (5) in the same way as described earlier, results in the inductor current (9) and discharge energy (10) dissipation

$$i_{\rm LR}(t) \approx -\frac{VDD}{\sqrt{\frac{L_{\rm R}}{C_{\rm iss}}}}e^{-\frac{R_{\rm G}}{2L_{\rm R}}t}\sin\left(\frac{1}{2}\sqrt{\frac{1}{L_{\rm R}C_{\rm iss}}}t\right) \tag{9}$$

$$\begin{aligned} E_{\rm dis_charge} &= \int_{t_5}^{t_6} R_{\rm G}i_{\rm LR}^2(t)dt \\ &= \int_0^{t_f} R_{\rm G}i_{\rm LR}^2(t)dt \\ &= \frac{\pi VDD^2R_{\rm G}C_{\rm iss}}{4Z_0}. \end{aligned} \tag{10}$$

Therefore, by using an $L-C$ resonant circuit topology and two clamp diodes, the power losses of the drive circuit are reduced to [15]

$$\begin{aligned} P_{\rm loss} &= (E_{\rm charge} + E_{\rm dis_charge})f_{\rm s} \\ &= \frac{\pi VDD^2R_{\rm G}C_{\rm iss}}{2Z_0} = \frac{\pi}{2}\frac{R_{\rm G}}{Z_0}Q_{\rm DD}VDDf_{\rm s}. \end{aligned} \tag{11}$$

Equation (11) establishes that, as the MOSFET gate resistance decreases, the power loss of the driver will also decrease. In the aforementioned analysis, it was assumed that all the energy used for the commutation would be recovered. In practice, the pMOS and nMOS in the "totem-pole" pair and the two blocking Schottky diodes lead to additional power losses; however, choosing pMOS and nMOS with a small on-resistance and two Schottky diodes with a small forward voltage and a small leakage current for $D_{\rm DR1}$ and $D_{\rm DR2}$ will make the relevant power loss as small as possible.

Switching loss: This drive circuit also reduces the switching loss of the device by adding the resonant inductor $L_{\rm R}$. During the turn on of M_1, the gate voltage $V_{\rm GS}$ charges up first. Once it reaches the threshold voltage, M_1 turns on, and the drain–source voltage of M_1, represented by $V_{\rm DS}$, decreases. Meanwhile, the drain current of M_1, represented by $I_{\rm d}$, increases. The turn-on switching loss occurs during this interval. When there is no resonant inductor, the drain current increases rapidly and reaches the output current before the drain–source voltage reaches zero, which produces a high overlap between $I_{\rm d}$ and $V_{\rm DS}$, leading to a significant switching loss. When the resonant inductor is added, the slew rate di/dt for M_1 decreases so that the drain current does not reach the output current when the drain–source voltage becomes zero. In this situation, the overlap between $I_{\rm d}$ and $V_{\rm DS}$ gets smaller so that the switching loss decreases. However, there is a tradeoff between the speed and the switching power loss, and the value of the inductor should be chosen carefully to satisfy the requirements of the drive circuit.

Cross-conduction loss: In the drive circuit, two separated small-width pulse signals are used to drive the pMOS and nMOS transistors in the "totem-pole" pair. Accordingly, there

Authorized licensed use limited to: University of South Carolina. Downloaded on February 15,2010 at 14:40:21 EST from IEEE Xplore. Restrictions apply.

is no chance for both the pMOS and nMOS transistors to be turned on at the same time. Consequently, the cross-conduction loss should be very small [15].

In summary, this resonant drive circuit reduces the conduction, switching, and cross-conduction losses so that the total gate-drive loss of the circuit is reduced.

IV. Design of the Drive Circuit for GaN HFETs

Section III explained that the resonant circuit with efficient energy recovery is a suitable drive circuit for high-frequency switches. This circuit also has the property of voltage clamping, which is required for driving GaN HFETs. However, this circuit is not directly applicable to HFET devices. In order to apply this topology to drive GaN HFETs, there are several problems that need to be considered.

1) GaN HFETs are zero-voltage turn-on devices. They require zero voltage to turn them on and a negative voltage to turn them off. Therefore, the drive circuit must be able to work under a negative voltage supply $VSSH$ and GND.
2) Most of the commercially available power MOSFETs have long delays and long rise and fall times; even the high-frequency power MOSFETs have rise and fall times of around 10 ns. For example, in the experimental tests described later, the nMOS transistor has 5-ns rise time, 5-ns fall time, and 8-ns turn-off delay time, while the pMOS transistor has 7-ns rise time, 10-ns fall time, and 11.2-ns turn-off delay time. Using a discrete power pMOS and nMOS as the "totem-pole" pair will add extra delay to the drive circuit and consequently limit the operation frequency of the drive circuit.
3) GaN HFETs operating above 10 MHz demand a high-speed drive circuit with an output current of about 50 mA. However, most of the commercially available power pMOS and nMOS transistors have much higher output-current rates which are not compatible with the GaN devices and lead to unnecessary power loss. For example, the output drive currents of pMOS and nMOS used for tests are around 1 A and are much bigger than the required drive current for the GaN HFET device desired to be driven. This high output current leads to high conduction energy dissipation, based on $E_{\mathrm{d}} = R_{\mathrm{on}} * I_{\mathrm{d}}^2$.
4) In the following application, the input control signals are 3.3-V low-power digital signals from digital systems, such as field-programmable gate arrays (FPGAs) and DSPs. Considering that the drive signal required for GaN HFETs is a signal with a voltage level from 0 to −7 V, an extra circuit needs to be added to change the polarity, voltage level, and current level of the input control signals.
5) A small-sized easily implemented drive circuit must be designed to fulfill the demand for convenient applications for GaN HFETs.

In order to drive the GaN HFET devices, the resonant drive circuit described in Section III was modified, as shown in Fig. 7.

As shown in Fig. 7, the drive circuit is working under a negative voltage $VSSH$. Two buffer stages were added to

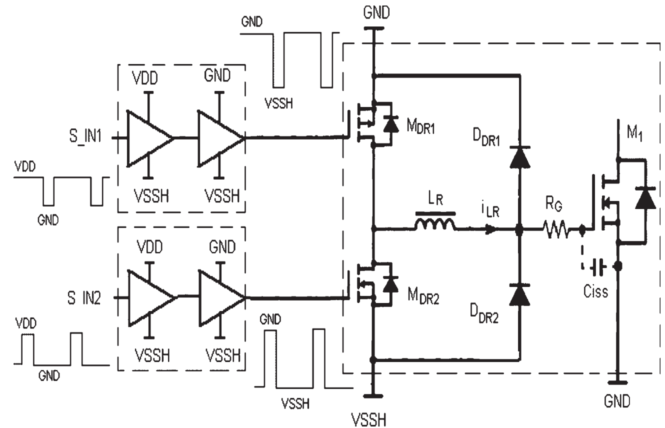

Fig. 7. Schematic of the proposed drive circuit for GaN HFETs.

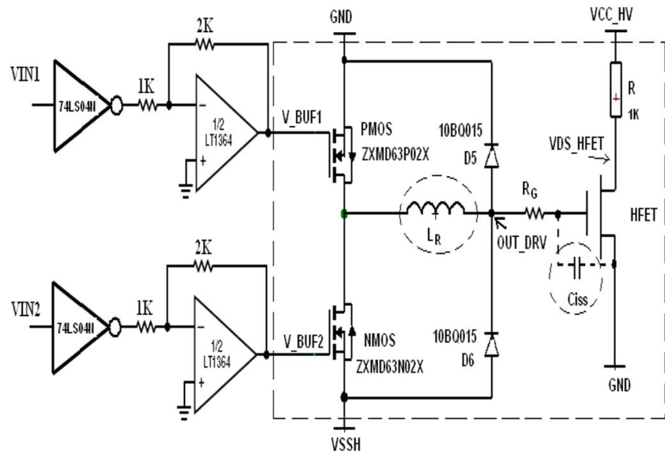

Fig. 8. Schematic of the topology implemented in the demonstrator.

change the polarity and the drive capability of the input control signals. The two amplified signals coming out of the buffer stages were used to drive the GaN HFET devices by means of the high-efficiency resonant driver which consists of a pair of high-speed low-loss pMOS, nMOS, two Schottky diodes, and a resonant inductor.

V. Simulation and Experimental Results

A. Design of the Prototype Board

In order to verify the topology of the drive circuit explained in Section IV, a prototype board realized with discrete components was built. Fig. 8 shows the complete schematic of the circuit implemented.

The input signals are two 3.3-V control signals coming from an FPGA board. The power supplies were chosen as $VDD =$ 3.3 V (see VDD in Fig. 7) and $VSSH = -7$ V.

Two high-speed operational-amplifiers (Op-Amps) LT1364 were used as the buffer stages to change the 3.3-V input control signals to −7-V signals with a higher drive capability.

In a real circuit, the on-resistances of the diodes and the transistors in the "totem-pole" pair lead to power loss in the driver. In order to reduce this type of power loss, low on-resistance transistors were chosen for the "totem pole," and Schottky diodes were used for D_5 and D_6 because they have

Authorized licensed use limited to: University of South Carolina. Downloaded on February 15,2010 at 14:40:21 EST from IEEE Xplore. Restrictions apply.

low forward voltages and small reverse-recovery charges. In the prototype board, a pair of low on-resistance high-frequency transistors (ZXMD63P02X and ZXMD63N02X) and Schottky diodes (10bq015) were chosen for the supplementary drive and for the recovery path, respectively. In Fig. 8, L_{R} is the parasitic inductance of the interconnect wire, which can be changed by adjusting the length of the wire. C_{iss} is the input capacitance of the HFET device, and the load R is 1 kΩ.

The GaN HFET switches were produced in the microelectronic laboratory of the University of South Carolina (USC). In the experimental evaluation, 100-μm-wide AlGaN/GaN HFET devices, with a gate length of 2 μm, gate-to-drain distance of 10 μm, and gate-to-source distance of 2 μm, built on sapphire, were used with the resonant driver. The devices had a measured current density of 0.8 A/mm, breakdown voltage above 300 V, and dynamic on-resistance of around 5 m$\Omega \cdot$ cm^2. The devices were passivated with silicon nitride and had a field plate with an overhang length of 2 μm for the suppression of current collapse. Compared with the property of the drive circuit, the current level of the GaN device is low (0.1 A), and it is not a good choice for these experimental tests. However, this device was used because it was the only one available in our lab at the time. One-millimeter GaN devices with a 1-A current level are now being fabricated in the USC semiconductor lab, and these devices will be used for future tests.

B. Aim–Spice Simulation Results

The resonant drive circuit itself can work at very high frequencies since the gate capacitance of the GaN devices is small.

Aim–Spice simulation was run for the resonant circuit (the dashed block in Fig. 8) situated after the Op-Amps. Fig. 9 shows the simulation result for a 10-MHz switching frequency with a pulsewidth of 10 ns for the input control signals.

In Figs. 8–10, VIN1 and VIN2 are the two input small pulsewidth control signals, V_BUF1 and V_BUF2 are the two signals which come out of the Op-Amps, and OUT_DRV is the gate–source drive signal for GaN HFET. Referring to the input control signals (VIN1 and VIN2) from the FPGA board, the delay time is around 8 ns; the rise time t_{r} is about 3 ns, and the fall time t_{f} is about 3 ns when the HFET device is loaded by a 1-kΩ resistor. The power loss of the drive circuit is 1 W, while the power loss for a traditional driver is 15.1 W.

The Aim–Spice simulation waveforms for the entire circuit are shown in Fig. 10.

As shown in Fig. 10, the delay time is 20 ns referring to the input signals (VIN1 and VIN2), the rise time is 8 ns, and the fall time is 8 ns. All of these values are much larger than those shown in Fig. 9. The main reason is the mismatch between the Op-Amps and power transistors in the "totem-pole" arrangement. Two high-speed Op-Amp chips LT1364 were used as the buffer stages. Considering that the output currents of this Op-Amp are approximately 50 mA, which is not large enough to drive the power transistors pMOS and nMOS in the "totem-pole" arrangement, the drive signals (V_BUF1 and V_BUF2 in Fig. 10) from the Op-Amp are distorted. These distorted signals, as well as the power MOSFETs themselves, lead to longer delay, rise, and fall times for the output gate–source switch signal shown in Fig. 10, compared with the simulation results shown in Fig. 9.

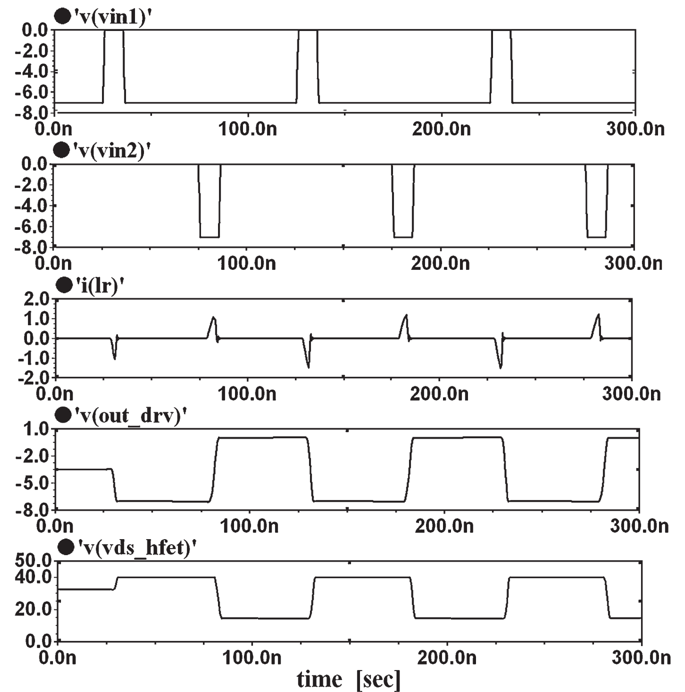

Fig. 9. Aim–Spice simulation waveforms of the dashed block in Fig. 8. Reference is made to 10-MHz switching frequency.

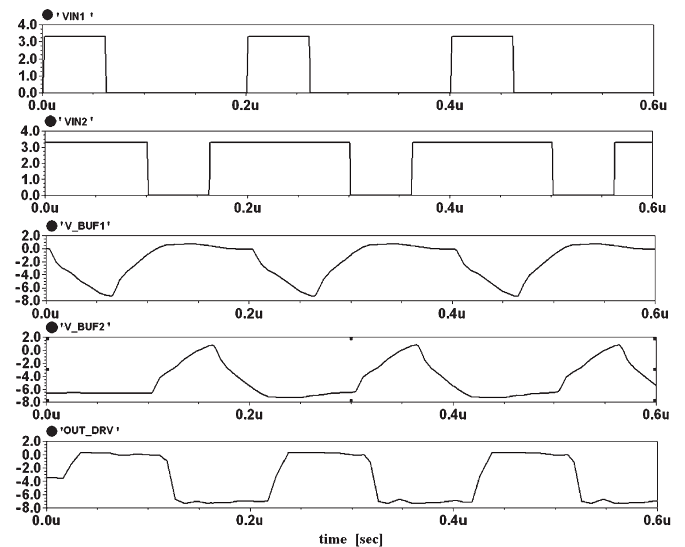

Fig. 10. Spice simulation waveforms for the whole drive circuit shown in Fig. 8.

C. Experimental Results

The testing waveforms for the complete circuit in Fig. 8 are shown in Fig. 11 which demonstrates the experimental waveforms with switching frequencies of 1, 2, and 5.55 MHz.

The input signals are at a voltage level of 3.3 V. As shown in Fig. 11, the drive circuit shifts the output voltage level and generates the 0−7-V gate–source switch signal for the GaN HFET switch.

Authorized licensed use limited to: University of South Carolina. Downloaded on February 15,2010 at 14:40:21 EST from IEEE Xplore. Restrictions apply.

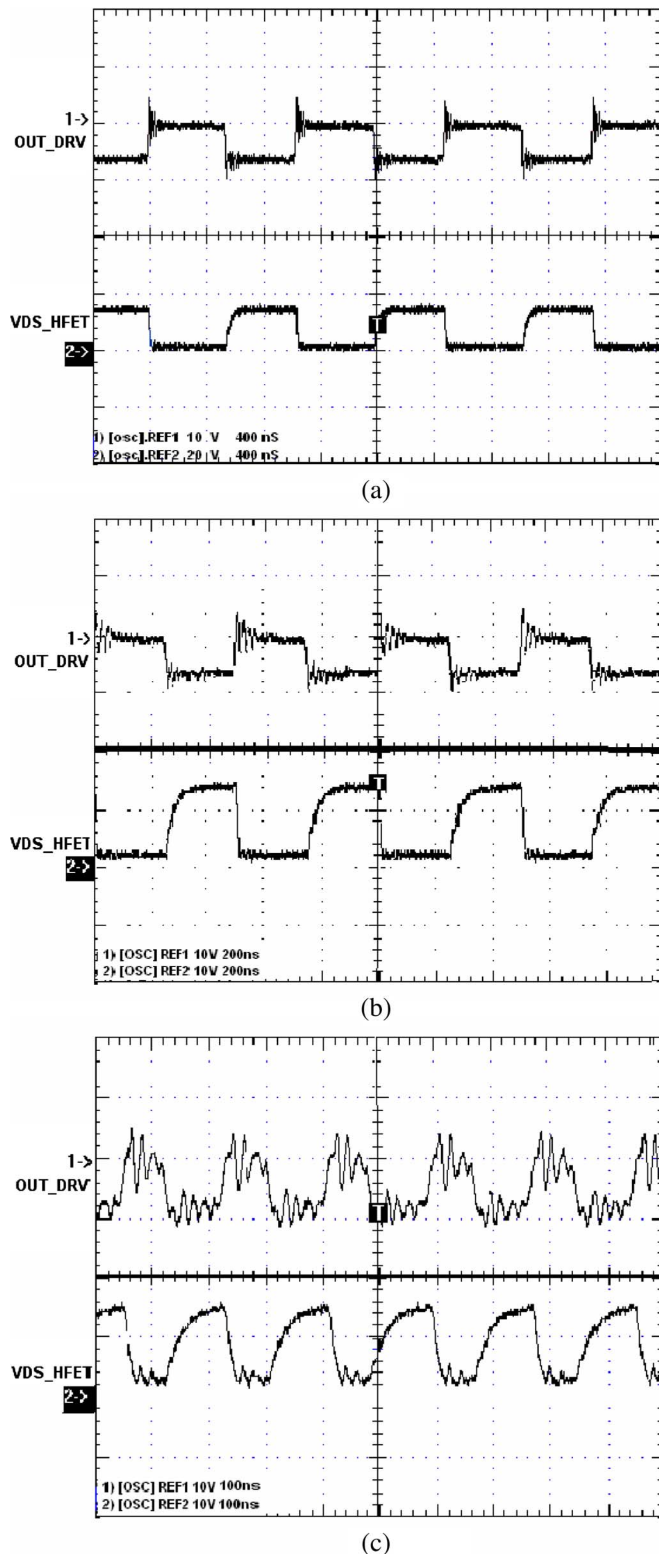

Fig. 11. Experimental measurements of the drive circuit demonstrator: with reference to (a) 1 MHz, (b) 2 MHz, and (c) 5.55 MHz.

Implementing this circuit with the prototype board presented several problems.

1) The experimental waveforms show the distorted signals due to the device mismatch described earlier. These distorted signals and the big power devices lead to large delay, rise, and fall times, as well as limit the operation frequency of the circuit. As shown in Fig. 11(a), for the 1-MHZ switching frequency, the rise and the fall times are both about 10 ns for the gate–source voltage of the GaN HFET.
2) Fig. 11 shows significant ripples on the gate–source voltage of the GaN device. The ripples are ascribable to the large parasitic inductors in the test circuit. In the prototype board, several different voltage supplies were used for different chips. In order to reduce the noise induced by these voltage supplies, each part of the circuit was situated far from each other. This leads to a parasitic inductance much bigger than that required for the LC tank. Furthermore, in these experimental tests, a long cable with large parasitic inductance was used to connect the drive circuit board and the GaN HFET because of the lack of the packaged GaN devices. These parasitic inductors together produce significant ripples on the gate–source voltage waveforms with the high frequencies shown in Fig. 11. The same value as these parasitic inductors was used to perform the Spice simulation, yielding the same results as the experimental tests (Fig. 12).

   In order to solve the problem brought by the unpackaged GaN devices and to better verify our topology of the drive circuit, a high-speed p-channel MOSFET (ZVP3310F), with 40-pF input capacitance, was chosen to repeat the same tests as those we did for GaN HFETs. The experimental results (shown in Fig. 13) are much better than those in Fig. 11. The ripples were reduced in Fig. 13 since the big parasitic inductance corresponding to the long interconnect cable was removed.
3) Another difficulty is due to the mismatch between the output properties of the power MOSFETs in the drive circuit and the drive GaN devices. The output drive current of the driver is too large for the GaN devices.

VI. Improvement of the Drive Circuit: Design of the Intergrated Circuit

In order to solve all the problems listed earlier, an integrated drive circuit is introduced in this paper. The entire drive circuit is implemented in a single integrated-circuit (IC) chip using Smart-Voltage-eXtension (SVX) technology, which builds HV devices in standard CMOS technologies by combining the existing layers without modification of the process steps.

Fig. 14 shows the schematic of the driver IC circuit for GaN HFETs, including the level shifters, charge pump, digital block, and resonant driver. The operation of the chip is as follows. The charge-pump circuit generates the negative high voltage $VSSH$ required for the resonant driver, from the positive low-voltage power supply VDD. Initially, the digital block converts the 3.3-V high-speed control signal, which is from digital systems (i.e., FPGAs, DSPs), into two narrow pulsewidth control signals in order to reduce the cross-conduction loss of the drive circuit. Next, the level shifters change the polarity of the control signals, with a corresponding increase in the voltage and power levels; the amplified signals are used to drive GaN HFETs by

Authorized licensed use limited to: University of South Carolina. Downloaded on February 15,2010 at 14:40:21 EST from IEEE Xplore. Restrictions apply.

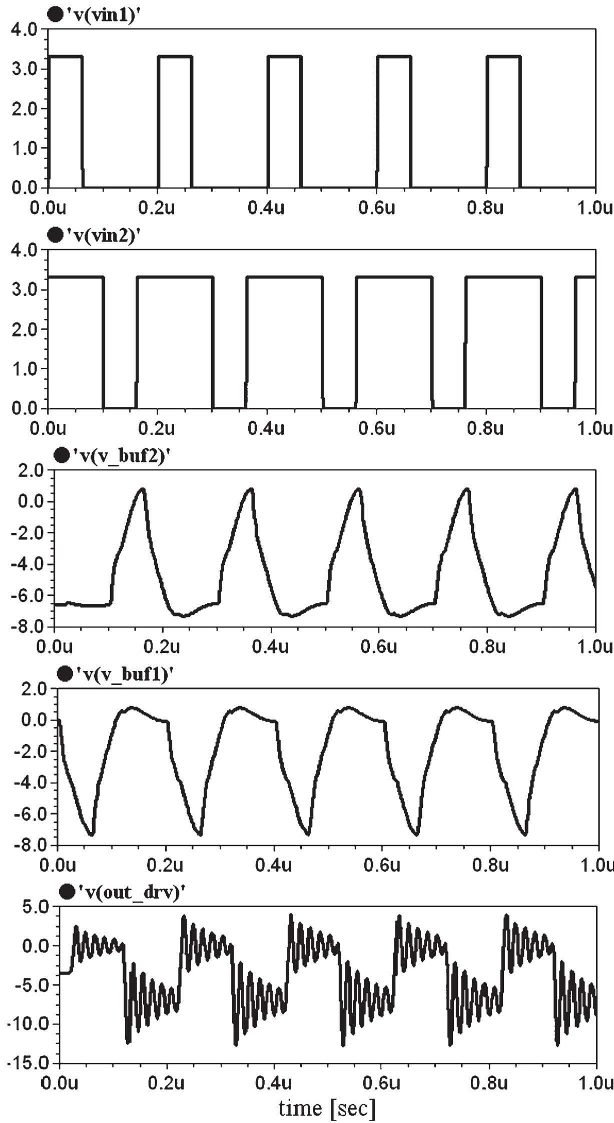

Fig. 12. Aim–Spice simulation results with the parasitic inductor for the cable.

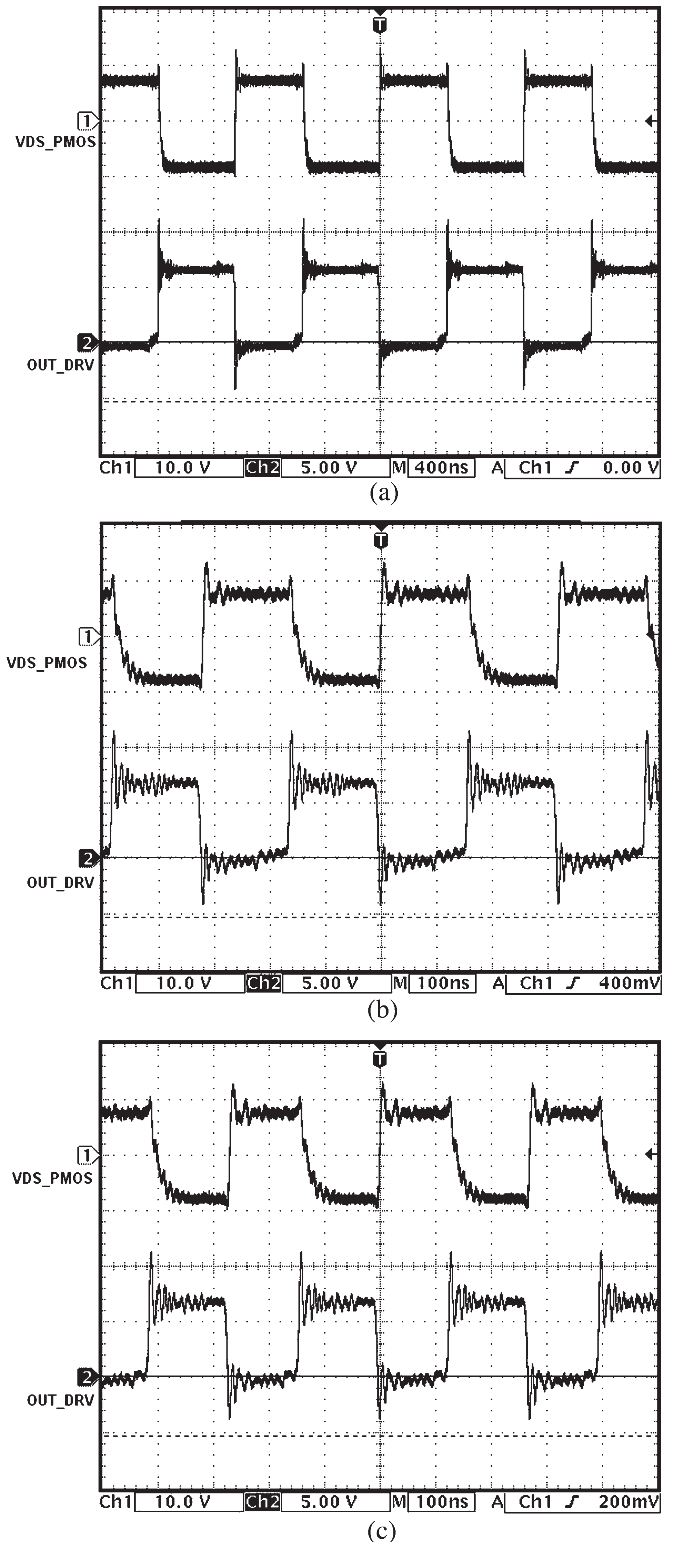

Fig. 13. Experimental measurements with P-channel MOSFET, with reference to (a) 1 MHz, (b) 3 MHz, and (c) 4 MHz.

means of a small-loss resonant circuit with efficient energy recovery described in Section III.

The resonant topology is constituted by the HV nMOS and HV pMOS connected in a "totem-pole" pair configuration, which will generate suitable current for GaN HFET. Proper values of L_{R}, obtained by adjusting the length of the printed circuit board (PCB) wire, and the C_{iss} of GaN HFETs govern the resonant transition.

In the CMOS process, the functions of the drain and the source on a transistor switch places, so to speak, if the polarity of their voltage changes. Thus, in the resonant driver, in order to avoid the improper operation of the transistors, diodes D_1 and D_2 are connected to the pMOS and nMOS to make them conduct unidirectionally. The body diodes of the pMOS and nMOS are always inverse biased to guarantee the proper operation of the devices; thus, diodes D_3 and D_4 are used, together with D_5 and D_6, to form the low-impedance path in order to recover the energy. Since the bond wire and the package of the IC chip contribute to a large part of the parasitic inductance, two discrete Schottky diodes were used for the blocking diodes D_5 and D_6, and placed as close as possible to the gate of the GaN devices. These diodes lead to additional power loss. However, this power loss is small because of the following reasons: the short time during which the current flows through the diodes to recover the energy, the small peak current

Authorized licensed use limited to: University of South Carolina. Downloaded on February 15,2010 at 14:40:21 EST from IEEE Xplore. Restrictions apply.

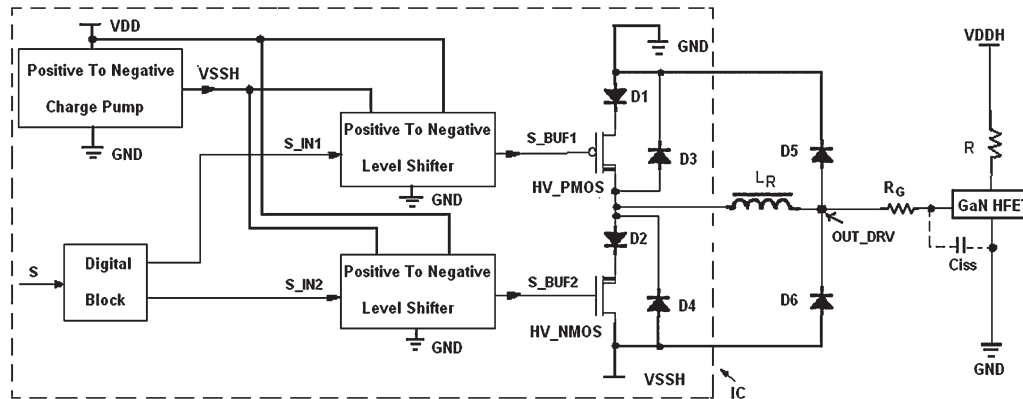

Fig. 14. Schematic of the IC of the driver IC for GaN HFETs.

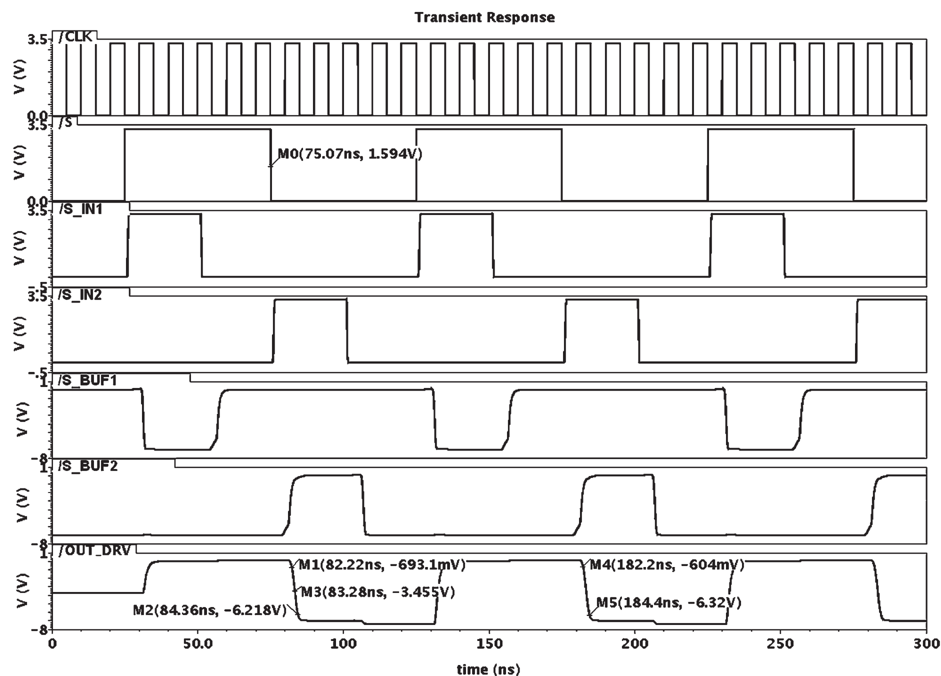

Fig. 15. Cadence–IC simulation waveforms of the circuit shown in Fig. 12 with reference to 10-MHz switching frequency.

(50 mA) of the diodes, and the small forward voltage (300 mV) and small leakage current for the Schottky diodes chosen for D_5 and D_6.

VII. Cadence-IC Simulation Results

The schematic and layout for the driver circuit shown in Fig. 14 is being built using Cadence-IC and other IC design tools. The process H35B4 in Austriamicrosystems was selected for the design. The simulation for the design of the driver is shown in Fig. 15, where the prelayout simulation results for a 10-MHz switching frequency with a pulsewidth of 30 ns for the input control signals is shown. In the simulation, the parasitic capacitances of all the components, except for the wire traces, are included. The input signals are 3.3-V LV signals, and the voltage swing of the output signal is from -7 to 0 V. For the simulation, the output drive current is about 50 mA. The rise time is about 2.5 ns, the fall time is nearly 2.5 ns, and the delay time is around 8 ns. The total power loss for the drive circuit is 198 mW.

VIII. Advantages of the New Resonant Driver for GaN HFET Switches

The proposed gate driver is specifically designed for GaN HFETs and has several advantages over the conventional solution. These advantages are listed as follows.

1) The drive circuit uses the topology of the resonant circuit with effective energy recovery, which has the advantages of low gate-drive loss, fast switching speed, voltage clamping, small cross-conduction power loss, and high tolerance of timing variation of the control signals [15].
2) SVX is used to implement the integrated drive circuit so that, instead of discrete power MOSFETs, HV nMOS and pMOS are used for the "totem-pole" pair in the resonant drive circuit. The sizes of the HV transistors can be carefully chosen to obtain a good match between the driver and the GaN devices and also to reduce the time delay induced by the drive circuit.
3) Using a parasitic inductor as the inductor in the LC tank allows the circuit to operate free of magnetic components.

Authorized licensed use limited to: University of South Carolina. Downloaded on February 15,2010 at 14:40:21 EST from IEEE Xplore. Restrictions apply.

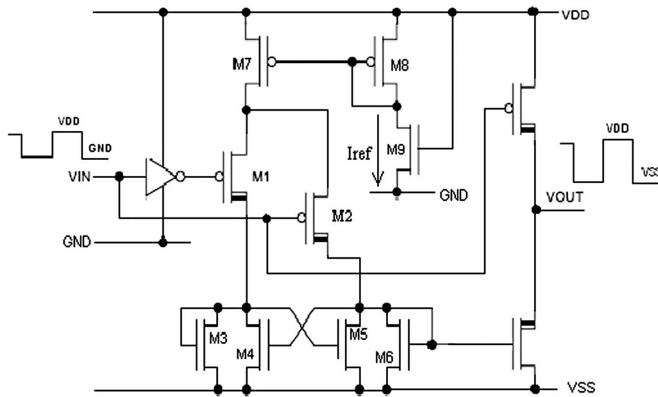

Fig. 16. Level shifter cell.

For GaN-based HFET switches, the input capacitor is small so that only a small inductor (1–20 nH) is required in this circuit. Typically, an inch of PCB conductor has an inductance of 15 nH. It is possible to take advantage of this kind of parasitic inductance in the circuit and obtain the inductance required for the LC tank by adjusting the length of the PCB wire between the drive circuit and the GaN device.

4) The level shifter changes the polarity and increases the voltage level and drive capability of the input signals. Fig. 16 shows a proposed circuit for a basic level-shifter cell [16].
5) The design of the integrated drive circuit reduces the size of the driver and also makes the application of GaN HFETs convenient.
6) Decreasing the parasitic resistance of the GaN HFET switch reduces the power loss of the drive system. The GaN HFET switch discussed in this paper is designed and fabricated at USC. Progress is still being made to improve the characteristics of these devices, for example, to reduce the parasitic gate resistance and, thus, the power loss.

IX. Future Work

Fabricating the IC for the proposed drive circuit is in progress at the Microelectronic Laboratory of USC. Further improvements in the circuit will be considered. The packaged GaN HFETs will be made in the USC semiconductor lab for testing.

X. Conclusion

The requirement for driving GaN HFETs and the design of the gate-drive circuit have been discussed in this paper. The presented topology provides a practical solution for the design of a high-speed gate driver for the GaN-based HFETs. The circuit also benefits from the use of GaN as a superior material in power electronics converters. Experimental results based upon a demonstrator confirm the efficiency of the resonant strategy used and the possibility of reaching high switching frequencies.

References

[1] M. A. Khan, G. Simin, S. G. Pytel, A. Monti, E. Santi, and J. L. Hudgins, "New developments in gallium nitride and the impact on power electronics," in *Proc. IEEE Power Electron. Spec. Conf.*, Recife, Brazil, 2005, pp. 15–26.
[2] N. Tipirneni, A. Koudymov, V. Adivarahan, J. Yang, G. Simin, and M. A. Khan, "The 1.6-kV AlGaN/GaN HFETs," *IEEE Electron Device Lett.*, vol. 27, no. 9, pp. 716–718, Sep. 2006.
[3] G. Simin, A. Tarakji, X. Hu, A. Koudymov, J. Yang, M. Asif Khan, M. S. Shur, and R. Gaska, "High-temperature performance of AlGaN/GaN metal–oxide–semiconductor heterostructure field-effect-transistors," *Phys. Stat. Sol. (A)*, vol. 188, no. 1, pp. 219–222, 2001.
[4] M. A. de Rooij, J. T. Strydom, J. D. van Wyk, and P. Beamer, "Development of a 1 MHz MOSFET gate-driver for integrated converters," in *Conf. Rec. 37th IEEE IAS Annu. Meeting*, 2002, pp. 2622–2629.
[5] "2.0A gate drive optocoupler with integrated (VCE) desaturation detection and fault status feedback," *Hewlett Packard Technical Datasheet for the HCPL316J Integrated Circuit*.
[6] "High and low side driver," *International Rectifier Technical Datasheet for the IR2113 Integrated Circuit*.
[7] "IGBT-driving hybrid ICs (EXB8.-series)," *Fuji Electric Application Manual*.
[8] "Hybrid Dual MOSFET-Driver," *Semikron Technical Datasheet for the SKHI 21 A Hybrid Gate Driver Circuit*.
[9] *Datasheet of DS0026*, Nat. Semicond., Santa Clara, CA, Feb. 2002.
[10] *Datasheet of LM5112*, Nat. Semicond., Santa Clara, CA, Oct. 2004.
[11] *Datasheet of UCC27323/4/5*, Texas Instrum., Dallas, TX, 2007.
[12] J. T. Strydom, M. A. de Rooij, and J. D. van Wyk, "A comparison of fundamental gate-driver topologies for high frequency applications," in *Proc. IEEE APEC*, 2004, pp. 1045–1052.
[13] Y. Chen, "Resonant gate drive techniques for power MOSFETs," M.S. thesis, Virginia Polytech. Inst. State Univ., Blacksburg, VA, 2000.
[14] I. D. de Vries, "A resonant power MOSFET/IGBT gate driver," in *Proc. IEEE APEC*, Mar. 10–14, 2002, vol. 1, pp. 179–185.
[15] Y. Chen, F. C. Lee, L. Amoroso, and H.-P. Wu, "A resonant MOSFET gate driver with efficient energy recovery," *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 470–477, Mar. 2004.
[16] H. Ballan, "High-voltage devices and circuits in standard CMOS technologies," Ph.D. dissertation, EPFL, Lausanne, Switzerland, 1997.

Bo Wang (S'00–M'05) received the B.S. and M.S. degrees in electrical engineering from Nanjing University of Science and Technology, Nanjing, China, in 1999 and 2002, respectively. Since 2005, she has been working toward the Ph.D. degree in the Department of Electrical Engineering, University of South Carolina, Columbia.

From 2002 to 2004, she was a Digital Integrated-Circuit (IC) Design Engineer with the Transportation and Standard Product Group, Semiconductor Product Section, Motorola Electronics, Ltd., Suzhou, China. Her research interests include IC design and power electronics. In particular, she is interested in mixed-signal IC design and gate-drive design for power devices.

Naveen Tipirneni (M'07) received the B.Tech. degree in electrical and electronics engineering from Jawaharlal Nehru Technological University, Hyderabad, India, in 2001, and the M.S. and Ph.D. degrees in electrical engineering from the University of South Carolina, Columbia, in 2003 and 2007, respectively.

He is currently a Staff Design Engineer with the Advanced Technology and High Voltage MOSFET Group, Vishay Siliconix, Santa Clara, CA. His research interests include employing novel physical and electrical properties of new materials to come up with environmentally friendly electronic devices. He shows extended interest in understanding device and material issues with wide bandgap semiconductors, such as SiC and (In, Al, Ga) III-N material systems for making efficient power electronic switches.

Authorized licensed use limited to: University of South Carolina. Downloaded on February 15,2010 at 14:40:21 EST from IEEE Xplore. Restrictions apply.

Marco Riva (M'99) received the M.S. degree in electrical engineering and the Ph.D. degree from the Politecnico di Milano, Milan, Italy, in 1994 and 1997, respectively.

From 1994 to 1997, he was with the Power Electronics and Electrical Drives Laboratory, Department of Electrical Engineering, Politecnico di Milano, where his research activity was mainly addressed in the field of electronic converters' analysis and control system optimization. Since 1998, he has been with Electronic Laboratory, Department of Physics, Università degli Studi di Milan, Milan, where he is currently an Assistant Professor. He is the author or coauthor of about 70 scientific papers and holds three patents. His research topics include modeling and design innovation of high-frequency converters, in both low- and high-voltage ranges, and design and stability analysis of high-efficiency and low-weight power converters, most frequently addressed to onboard space satellite electronic systems and equipment.

Dr. Riva serves on the Administration Committee of the Italian Association of Electrical, Electronic and Telecommunication Engineers (AEIT-Federazione Italiana di Elettrotecnica, Elettronica, Automazione, Informatica e Telecomunicazioni) and on the Technical Committee 22 (Power Electronics) of the Italian institution for technical standards in the electrical, electronic, and telecommunication fields (CEI-Comitato Elettrotecnico Italiano). He is also a member of the Italian Association for Automation (ANIPLA-Associazione Nazionale Italiana per l'Automazione) and of the IEEE Power Electronics and IEEE Industrial Electronics Societies.

Antonello Monti (S'88–M'89–SM'02) received the M.S. degree in electrical engineering and the Ph.D. degree from the Politecnico di Milano, Milan, Italy, in 1989 and 1994, respectively.

From 1990 to 1994, he was with the Research Laboratory, Ansaldo Industria, Milan, where he was responsible for the design of the digital control of a large power cycloconverter drive. He became an Assistant Professor with the Department of Electrical Engineering, Politecnico di Milano, in 1995. Since August 2000, he has been an Associate Professor with the Department of Electrical Engineering, University of South Carolina, Columbia. He is currently the Director of the Institute for Automation of Complex Power Systems, E.ON Energy Research Center, RWTH Aachen University, Aachen, Germany. He is the author or coauthor of more than 200 papers in the fields of power electronics and electrical drives.

Dr. Monti served as the Chair of the IEEE Power Electronics Committee on Simulation, Modeling, and Control and as an Associate Editor of the IEEE TRANSACTIONS ON AUTOMATION SCIENCE AND ENGINEERING.

Grigory Simin (A'01–M'03–SM'03) received the M.S.S.E. degree from Leningrad Electrotechnical Institute, Leningrad, Russia, in 1971, the Ph.D. degree in physics of semiconductors and dielectrics from Giricond Science and Research Institute, Leningrad, and the Senior Research Scientist Diploma from the Supreme State Committee on Academic Degrees in 1985, where, during this period, his research included Gunn effect devices, GaAs metal semiconductor field-effect transistors, microwave and optical integrated circuits (ICs), and semiconductor lasers.

Since 2001, he has been an Associate Professor with the Department of Electrical Engineering, University of South Carolina, Columbia. His research interests include GaN-based electronic devices and monolithic microwave ICs. He has published four books, several book chapters, and more than 150 articles in refereed journals.

Enrico Santi (S'91–M'93–SM'01) received the Dr.Ing. degree in electrical engineering from the University of Padua, Padova, Italy, in 1988, and the M.S. and Ph.D. degrees from the California Institute of Technology, Pasadena, in 1989 and 1994, respectively.

From 1993 to 1998, he was a Senior Design Engineer with TESLAco, Irvine, CA, where he was responsible for the development of various switching power supplies for commercial applications, such as dc–dc power converters for telecommunications, and fluorescent light electronic ballasts for avionic applications. Since 1998, he has been with the University of South Carolina, Columbia, where he is currently an Associate Professor in the Department of Electrical Engineering. He has published over 90 technical papers and book chapters on power electronics and modeling and simulation and holds two patents. His current research interests include power electronics. Specifically, he is interested in physics-based modeling of power semiconductor devices, control of power electronics systems, modeling and simulation of advanced power systems, and development of hybrid power sources. He is involved in the development of the Virtual Test Bed.

Dr. Santi serves as an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS and of the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS. He is a member of the IEEE Power Electronics Society Administrative Committee, Faculty Advisor of the Student Chapter of the IEEE, and Chair of the Power Electronics Devices and Components Committee of the IEEE Industry Applications Society.

Authorized licensed use limited to: University of South Carolina. Downloaded on February 15,2010 at 14:40:21 EST from IEEE Xplore. Restrictions apply.