Power SiC DMOSFET Model Accounting for JFET Region Nonuniform Current Distribution

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***Abstract* - The main goal of this work is development of a new circuit-based SiC DMOSFET model which physically represents the mechanism of current saturation in power SiC DMOSFET. Finite element simulations show that current saturation for a typical device geometry is due to two-dimensional carrier distribution effects in the JFET region caused by the current spreading from the channel to the JFET region. For high drain-source voltages, most of the voltage-drop occurs in the current-spreading region located in the JFET region close to the channel.**

I. INTRODUCTION

For switching converter applications at less than 200V the silicon power MOSFET has become the device of choice due to its low on-state resistance and fast switching speed. When designed for higher operating voltages, the use of silicon MOSFETs becomes impractical due to the very high drift region resistance. For higher blocking voltages, IGBTs and GTOs are commonly used. However, these devices have relatively high on-state voltage drop and relatively slow switching speed. Excellent electrical properties of silicon carbide (SiC) material make it a very attractive semiconductor material for power switching devices with capabilities that are superior to those of devices based on silicon technology. In particular, 4H-SiC MOSFET is one of the most promising candidates for high-speed and low-loss power switching applications.

Thanks to recent progress in SiC technology [1], [2], SiC MOSFETs are on the verge of commercialization. Since SiC MOSFETs are still under development, there is a need to create accurate models for SiC prototype devices so that engineers can explore through circuit-level simulation the advantages that the introduction of these devices can provide in their switching converter designs.

Device models can be divided in two major groups: **1)** analytical models based on the finite element solution of drift-diffusion carrier transport in two or three dimensions; and **2)** circuit-oriented models which employ equation-based description of device behavior. Analytical models provide very high accuracy but require long simulation time and detailed information about device fabrication, while circuit-based models require much less time for simulation with acceptably accurate results using model parameters that can be extracted from experimental measurements. An additional advantage of circuit-oriented models is that they are compatible with circuit simulators and can be used to simulate an entire switching converter. While extensive research has been done to develop analytical models for SiC MOSFET [3]-[5], there are very few publications addressing the implementation of circuit-oriented models in simulators such as PSpice [6], [7].

II. FINITE ELEMENT SIMULATION

Typical structure of a power SiC DMOSFET is shown in Fig.1. The physical dimensions and doping concentrations are for a 1.2kV device. Applying a positive voltage to the gate larger than the threshold voltage, a deep inversion layer is created on top of the p-base region, forming an n-type conducting channel connecting the source to the drain region. At the same time, an accumulation layer is formed under the gate oxide at the top of the JFET region, providing current spreading for the electron current flowing from the channel into the JFET region. For small values of drain-source voltage, the device exhibits an approximately constant on-state resistance, which is determined by channel and drift region resistances. Ultimately, at a higher drain-source bias, the current saturates. From standard analysis of power MOSFETs, it is known that there are two possible mechanisms of current saturation in power MOSFET: channel pinch-off or carrier velocity saturation, whichever occurs first. According to performed finite element simulations, carrier velocity saturation is the reason for current saturation for the SiC DMOSFET structure of Fig. 1.

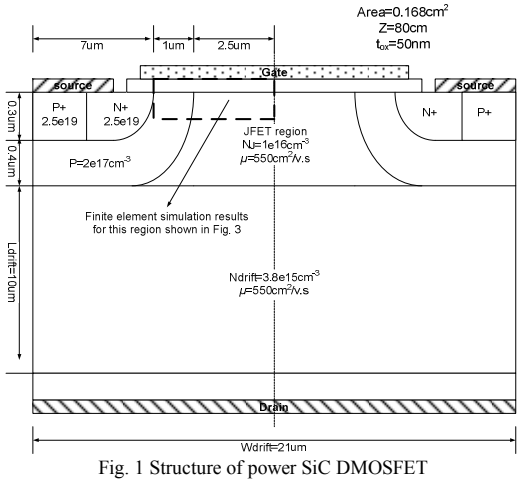


Fig. 1 Structure of power SiC DMOSFET

Fig.2 shows the forward I-V characteristic obtained from finite element simulation using Silvaco ATLAS. Gate voltage is constant (7V) for all drain-source voltages, ensuring the deep inversion of the modulated channel. Fig.3 shows finite element simulation results of the upper part of the DMOSFET (rectangular dashed region in Fig. 1). The figure shows finite element simulations of potential and current transport in SiC DMOSFET for conditions corresponding to saturation regime at V_{ds}=5V. This corresponds to the rightmost point in the forward characteristic of Fig.2. Fig.3(a) shows the two-dimensional potential distribution and the potential curve on a cutline along the channel (cutline: X=7μm-10.5μm, Y=5nm) and Fig. 3(b) shows the two-dimensional current density distribution and the electric field curve along the same cutline (cutline: X=7μm-10.5μm, Y=5nm) obtained from finite element simulation. From these simulation results one can draw some conclusions on saturation mechanism in a typical power SiC DMOSFET. Pinch-off of the channel was not observed under any drain-source bias: even at V_{ds}=10V the channel retains its approximately rectangular shape and does not display channel pinch-off condition. Fig. 3(b) shows that the horizontal electric field goes to its maximum value E_m at the end of the channel (up to 2×10^5 V/cm). Detailed investigation of carrier transport in the channel region reveals carrier velocity saturation is responsible for current saturation.

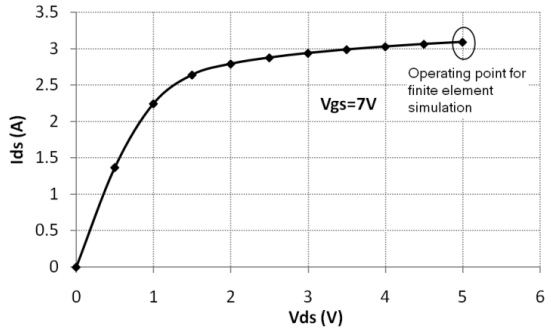
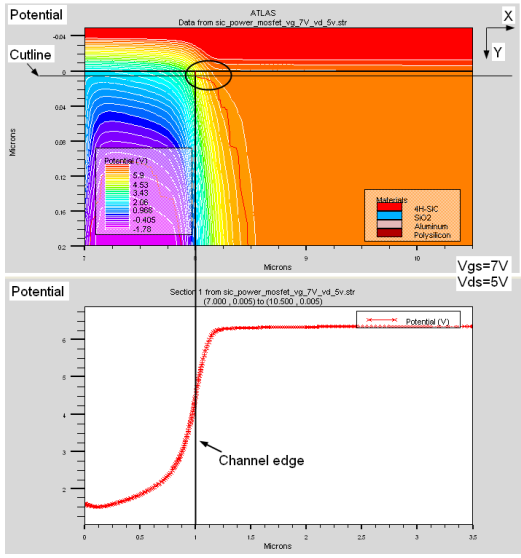
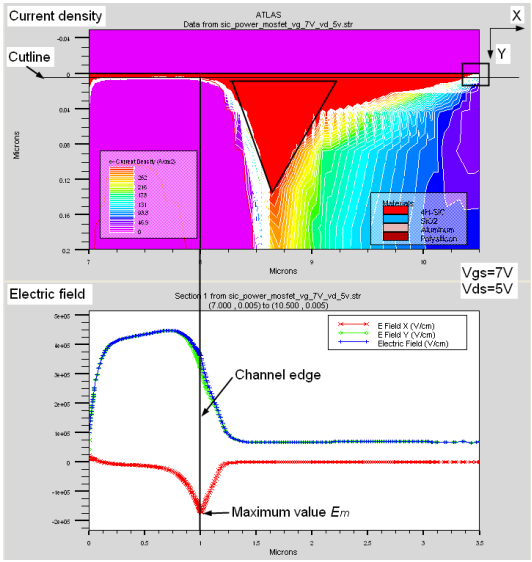


Fig. 2 I-V characteristic of DMOSFET at Vgs=7V based of finite element simulation

Traditionally, it is assumed that an accumulation layer is always formed under the gate oxide in the JFET region and further analysis of current transport in power MOSFET is based on this assumption. This accumulation layer helps spreading the electron current coming from the channel uniformly across the undepleted portion of the JFET region. As a result, the JFET region can be represented as a rectangular piece of semiconductor material whose width is modulated by change of depletion region width of p-base/n-JFET junction, with electron current flowing vertically from the JFET accumulation layer under the gate to the drift region. However, the finite element simulations of Fig.3(b) tell a different story: even for small values of drain-source voltage, the current distribution in the JFET region is highly non-uniform and current crowding occurs in the region adjacent to the p-base/n-JFET junction depletion layer (see triangular region in Fig.3(b) for V_{ds} = 5V). Notice that the accumulation layer under the gate oxide in the JFET region tends to disappear in the mid-region between adjacent p-base regions (rectangular region in Fig. 3b). Notice also that the potential increases sharply at the end of the channel. Most of the voltage drop is localized in the current spreading region across the depleted portion of the JFET region (see circled region in Fig. 3a). So one can divide the JFET region into two parts: one is the current spreading region across the depleted portion, with electron current spreading out laterally; the other is the rectangular region mentioned before, with electron current flowing vertically and non-uniformly. Based on this idea, a new circuit-based model is developed, which physically represents the mechanism of current saturation in power SiC DMOSFET.



(a) Potential distribution and cutline



(b) Current density distribution and electric field cutline

Fig. 3 Finite element simulations of SiC DMOSFET

The physical treatment of current spreading in DMOSFET proposed by Baliga [8] considers accumulation and JFET region as two individual regions. Resistance of accumulation region is determined by gate voltage only, while resistance of JFET region is a function of drain-source voltage only. However, based on performed investigation, the resistance of accumulation region is a strong function of both V_{GS} and $V_{DS,}$ which is not considered in classical solutions for current transport of power DMOSFET. Moreover, the resistance of JFET region is not only determined by depletion width of p-base/JFET junction, but also and more predominantly by reduction of current conduction in the central part of JFET region caused by formation of a depletion region between adjacent p-base regions (rectangular region in Fig. 3b).

III. NOVEL MODEL WITH JFET REGION NONUNIFORM CURRENT DISTRIBUTION

Fig. 4 shows a simple standard model of power MOSFET with two different operating regions: linear region and saturation region. For simplicity device capacitances are not shown. When channel voltage $V_{CH} < V_{CH,SAT}$ (saturation voltage), drain current I_D is dependent on gate- source voltage V_{GS} and channel voltage V_{CH}. When $V_{CH} \geq V_{CH,SAT}$, I_D is a function of V_{GS} only and does not depend on V_{CH} . So there are two different equations for current I_D in the standard model.

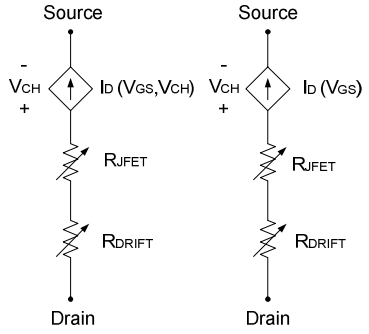


Fig. 4 Standard power MOSFET static model structure

The structure of the proposed model is shown in Fig. 5. It consists of voltage-controlled current source I_D, voltage source V_{J2}, JFET region resistance net R_{J_net}, drift resistance R_{DRIFT}, and capacitances C_{GS}, C_{GD} and C_{DS}. The novelty of this model is in how the JFET region is modeled by V_{J2} and R_{J_net}.

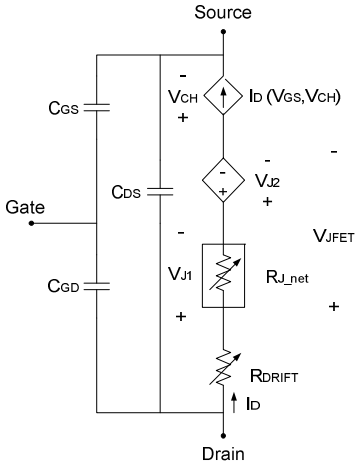


Fig. 5 Proposed SiC DMOSFET model structure

Taking into account that SiC MOSFET current saturation is due to a large voltage drop in JFET region and not to channel pinch-off, it is possible to use only one equation to describe the channel region forward I-V characteristic. This is the equation corresponding to linear region of operation in the standard model of Fig. 4:

$$I_D = \frac{\mu_{CH} C_{OX} Z}{2L_{CH}} \left[2(V_{GS} - V_T) V_{CH} - V_{CH}^2 \right] \quad (1)$$

Thus, channel region is represented by a voltage-controlled current source and channel voltage V_{CH} can be determined by subtracting voltage drop in JFET and drift region from total voltage applied to the device:

$$V_{CH} = V_{DS} - V_{JFET} - I_D R_{DRIFT} \quad (2)$$

where,

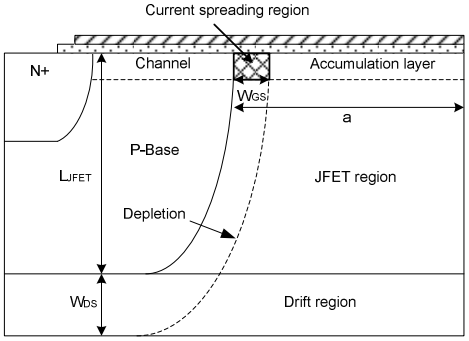
$$R_{DRIFT} = \frac{L_{DRIFT} - W_{DS}}{2 \cdot q \cdot \mu_{n-drift} \cdot N_{DRIFT} \cdot Z \cdot W_{DRIFT}} \quad (3)$$

$$W_{DS} = \sqrt{\frac{2\varepsilon_{sic}}{q \cdot N_{DRIFT}} (V_{bi} + V_{CH} + V_{JFET})} \quad (4)$$

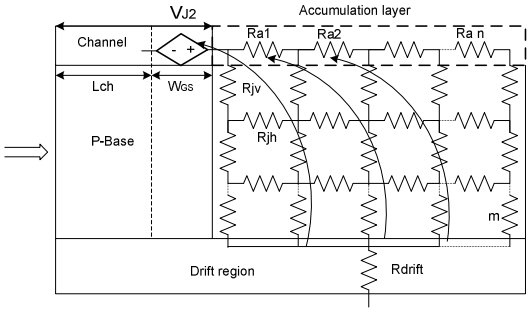
where V_{JFET} is the voltage drop in JFET region.

The proposed method to capture the current saturation in the discussed DMOSFET is to represent JFET region as two parts: a voltage source and a matrix of resistors as in Fig. 5. The specific structure is shown in Fig.6. Voltage source V_{J2} represents the voltage drop in the current spreading region and the resistor network allows for a non-uniform current distribution in the JFET region. This approach takes into account JFET region voltage drop in both lateral and vertical directions, therefore capturing the two-dimensional nature of current spreading in this region. The top row of resistors represents the accumulation layer while the remaining matrix resistors represent the main body of JFET region. The main feature of this approach is

that values of the resistors in the accumulation layer are function of both V_{GS} and V_{DS}. Let us consider a resistor R_{ai} in the top row. Due to the voltage drop on the resistors to its left, the voltage V_{Gai} between the gate and the resistor node *ai* is decreased, causing the reduction of accumulation layer thickness. As a result, it is $R_{a1} < \ldots < R_{ai} < R_{an}$. This effect contributes to current crowding at the depletion layer edge in the JFET region.



(a) Specific structure of channel and JFET region



(b) Circuit representation of JFET region

Fig. 6 Model description of JFET region

To model the voltage drop in vertical direction inside the JFET region, a resistor matrix with *n*-columns and *m*-rows is used. First top row of resistors R_{ai} represents accumulation region and can be expressed as:

$$R_{ai} = \frac{L_R}{Z\mu_A C_{OX}(V_{GS} - V_T - V_i)} \tag{5}$$

where μ_A is accumulation layer mobility, V_i is voltage at the node of corresponding *i* resistor and L_R is the distance between adjacent nodes:

$$L_R = \frac{a - W_{GS}}{n} \tag{6}$$

$$W_{GS} = \sqrt{\frac{2\varepsilon_{sic}}{q \cdot N_{JFET}}(V_{bi} + V_{CH} + V_{J2})} \tag{7}$$

When V_i is smaller than (V_{GS}-V_T), R_i has a positive value, representing the accumulation layer resistance. With V_i increasing, the voltage drop (V_{GS}-V_T-V_i) goes to zero and R_i tends to infinity. From a physical point of view, a depletion region forms, replacing the rightmost portion of the accumulation layer (rectangular region in Fig. 3b).

JFET region resistive net is represented by horizontal and vertical resistors (see Fig. 6(b)):

$$R_{jh} = \frac{L_R m}{q\mu_{JFET} N_{JFET} ZL_{JFET}} \tag{8}$$

$$R_{jv} = \frac{L_{JFET}}{q\mu_{JFET} N_{JFET} ZL_R m} \tag{9}$$

The voltage source V_{J2} represents the voltage drop in the current spreading region. It is a critical element in the proposed model, because when the current saturates, this portion supports the increased applied voltage. Since electric field reaches its maximum value E_m at the end of the channel and decreases linearly to 0 along W_{GS}, the voltage source can be described by

$$V_{J2} = \frac{1}{2} E_m W_{GS} \tag{10}$$

where the maximum electric field E_m can be obtained from

$$I_D = C_{OX}(V_{GS} - V_T - V_{CH}) Z \cdot \mu_{CH}(E_m) \cdot E_m \tag{11}$$

and the field-dependent carrier mobility at the end of the channel is given by

$$\mu_{CH}(E_m) = \mu_{CH0} \cdot \left[1 + \left(\frac{\mu_{CH0} E_m}{v_{sat}} \right)^{\beta} \right]^{-1/\beta} \tag{12}$$

where μ_{CH0} is the low-field mobility in the inversion layer and v_{sat} is the carrier saturation velocity. Because the maximum electric field E_m increases with increasing drain-source voltage, for low voltage V_{J2} is so small that it does not affect the linear region characteristic. But for high voltage, V_{J2} supports most of the applied voltage because of the strong electric field. As a result, the channel voltage V_{CH} reaches a constant maximum value and the device current also saturates. As a result, equation (1) describing the channel region is valid under all operating conditions.

IV. MODEL VALIDATION

The model is validated by comparison with finite element simulations and experimental measurements. A high power SiC DMOSFET from CREE inc., rated at 1200V 20A, is used for experimental validation. The device has similar design as the one shown in Fig.1. A full set of measurements is performed in order to assist model

adjustment and verification, including: static I-V characteristics, C-V characteristics and dynamic characterization under resistive switching conditions. Fig. 7 shows the comparison of C-V characteristics between experimental results and finite-element simulated results. Fig. 8 shows the comparisons of $1/(C_{ds}^2)$ and $1/(C_{gd}^2)$ versus drain-source voltage V_{ds}. Notice that the good matching of simulation data with experimental data at higher voltage. The offset in Fig.8(a) can be modified by slightly changing the p-base/n-JFET junction built-in voltage by adjusting carrier concentrations.

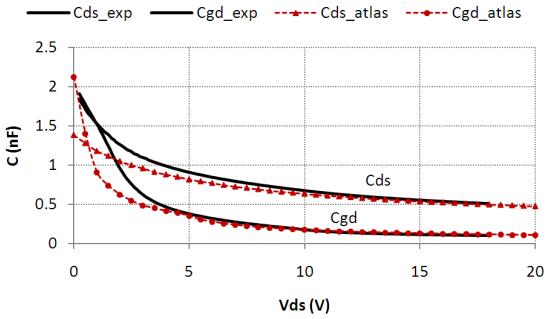
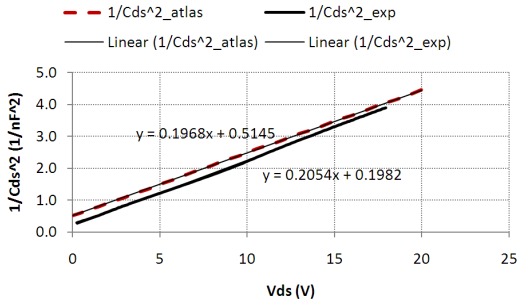
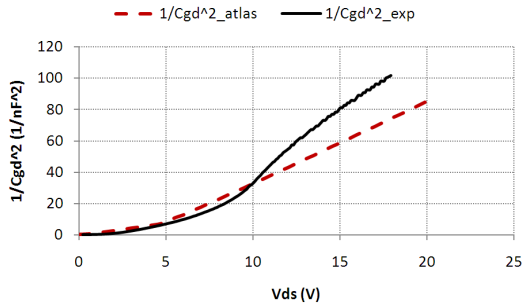


Fig. 7 Comparison of C-V measurements between experimental and finite-element simulated results



(a) $1/(C_{ds}^2)$ versus V_{ds}



(b) $1/(C_{gd}^2)$ versus V_{ds}

Fig. 8 Comparisons of experimental and simulated results of $1/(C^2)$ versus V_{ds}

Static forward characteristics were measured using a Tektronix 371A power curve tracer for four values of gate-source voltage: 7V, 11V, 15V, 19V. The experimental static characteristic of the device are compared with model predictions in Fig. 9. Static characteristics obtained using the standard model of Fig. 4 are included for comparison.

Fig. 10 shows simulated result of the current in the individual resistors of the accumulation layer as a function of drain-source voltage (shown for a four- column resistive net). As it can be seen, when drain-source voltage increases, current tends to flow through resistors that are closer to the channel. Fig. 11 and Fig. 12 show the channel voltage V_{CH} and current spreading region voltage V_{J2} in JFET region for V_{GS}= 7V, 11V, 15V and 19V. The forward characteristic for V_{GS}= 7V shown in Fig. 9 exhibits current saturation as voltage V_{DS} increases. Looking at Figs. 11-12 one can see that, as drain-source voltage increases, channel voltage tends to saturate while V_{J2} supports most of the voltage drop, and, as a result, device current saturates.

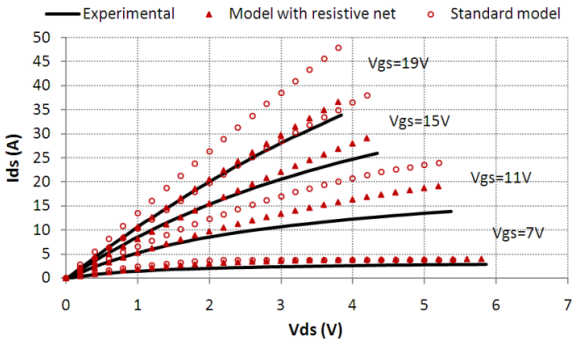


Fig. 9 Comparison of experimental and simulated forward characteristic of SiC DMOSFET

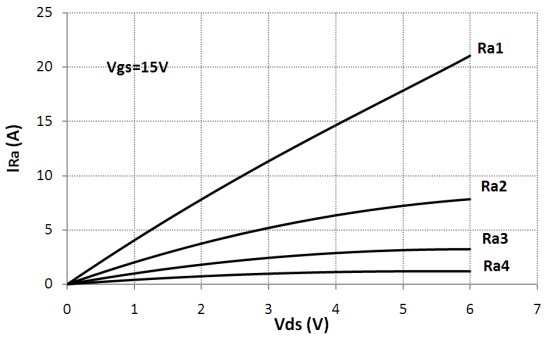


Fig. 10 Model current in accumulation resistors of SiC DMOSFET

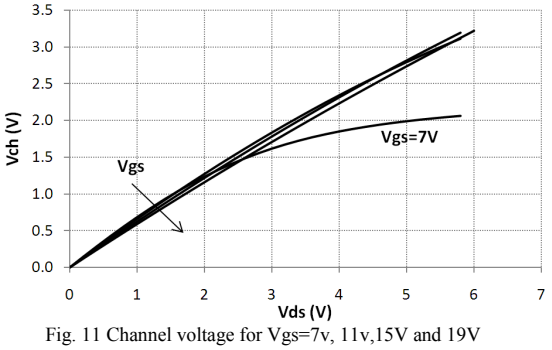


Fig. 11 Channel voltage for Vgs=7v, 11v,15V and 19V

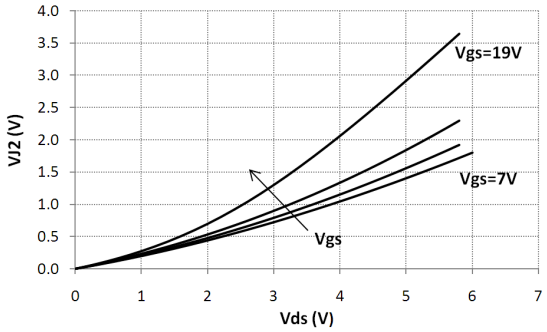


Fig. 12 Voltage source V_{J2} in JFET region for Vgs=7V, 11v,15V and 19V

A printed circuit board (PCB) testbed was built to perform resistive switching experiments on the SiC DMOSFET. Fig.13 shows the corresponding resistive switching circuit used in simulation, which includes parasitic inductors L_s, L_d and L_g. Inductor L_d represents the switching loop inductance. Inductor L_s is the MOSFET source-leg parasitic inductance and provides a feedback path from JFET drain current to gate-source voltage during transitions. Inductor L_g is the gate circuit loop inductance. Comparison between experimental and simulation results are shown in Fig. 14 for resistive turn-on and in Fig. 15 for resistive turn-off. The simulation results are in reasonably good agreement, even if there are some differences, especially in the waveforms of gate-source voltage V_{gs}. A possible explanation for the discrepancy is that in the current model implementation the MOSFET capacitances have a constant value, independent of applied voltages. An improved model version with voltage-dependent capacitances is currently under development.

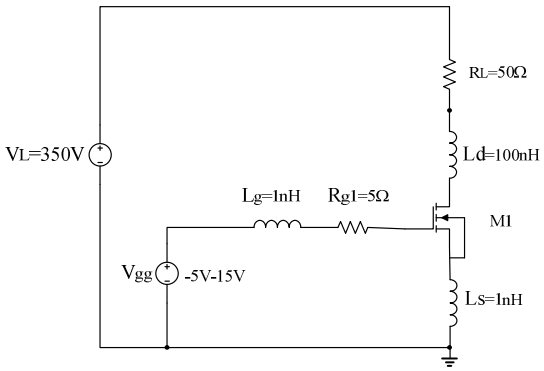


Fig. 13 Equivalent circuit used for resistive switching simulation using the proposed model

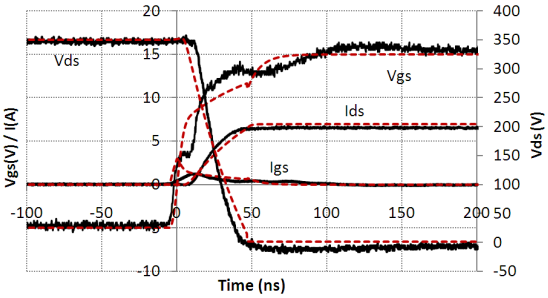


Fig. 14 SiC DMOSFET simulated (dashed) and experimental (solid) turn-on waveforms of resistive switching

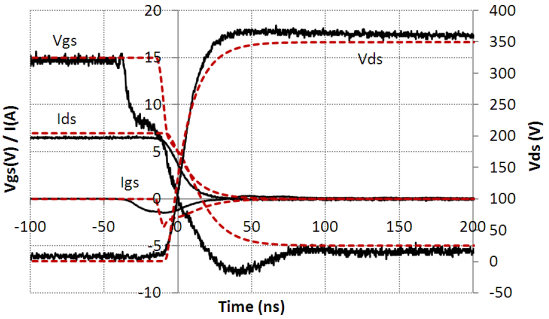


Fig. 15 SiC DMOSFET simulated (dashed) and experimental (solid) turn-off waveforms of resistive switching

V. CONCLUSION

A novel DMOSFET model has been proposed. The new feature of the model is that it provides a more physical description of the saturation phenomenon in power MOSFETs, which accounts for JFET region nonuniform current distribution. The physical basis of the proposed model is motivated by finite element simulations. The model is validated both statically and under resistive switching conditions for SiC DMOSFET showing overall good matching with experimental results.

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