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Abstract – In this paper, the interfacing schemes for Power-Hardware-in-the-Loop (PHIL) simulations are studied. In Part I, different simulation/hardware interfaces are introduced, and a novel interfacing scheme based on the time-variant first-order approximation of dynamics of the hardware under test (HUT) is proposed. The performances of different interfaces are compared through the decoupled simulation of first-order systems. More advanced performance evaluation methods are introduced in part II.

I. INTRODUCTION

Generally, there is only signal coupling between the hardware and the virtual system in HIL simulations. Therefore, HIL techniques are limited to control or low-power applications. PHIL, on the other hand, enables the natural coupling between the simulation software and the system hardware, hence greatly extending the applicability of the HIL experiments. In the PHIL simulation system, the simulation/hardware interface occurs at a connection where real power is virtually exchanged between the simulation software and the real hardware (in contrast to the usual case where the interface occurs at a signal connection). The structure of the PHIL system is shown in Fig. 1.

PHIL simulation significantly broadens the range of applicability of HIL technology. For example, it provides the opportunity to analyze how new equipment, such as a new motor, will affect a complex power system before installation of the real equipment. The key element in PHIL simulation is the simulation/hardware interface, which enables the natural coupling between the actual power hardware and the simulation software [1]. In this paper, different interfacing schemes are introduced and their performances are compared through the decoupled simulation of a simple first-order system.

II. SIMULATION/HARDWARE INTERFACES

A. The Simulation/Hardware Interface based on Ideal Transformer Model

The simulation/hardware interface based on ideal transformer model (ITM) uses the combination of two ideal controlled sources to enforce the conservation of energy [2]. From the software standpoint, this interfacing scheme has two configurations. Both configurations can be described as an ideal transformer: in one case the virtual side of the interface behaves as a voltage-controlled current source as shown in Fig. 2, and in the other as a current-controlled voltage source as shown in Fig. 3. The first configuration of the interface is applied when the HUT appears to be inductive under the main operation frequency, while the second one is for capacitive HUT. When the load is purely resistive, both configurations are applicable.

B. The Simulation/Hardware Interface based on Transmission Line Model

The transmission line modeling (TLM) technique models the discrete reactive components as transmission-line sections, which are known as TLM links [3]. Consider a system that consists of two circuits connected through a reactive component (either a capacitor or an inductor), as shown in Fig. 4.

If each reactive component is treated as a two-port device and the voltage change in a capacitor or the current change in an inductor within each simulation time step are very small, then circuit A and B can be considered as being connected to a constant voltage or current source, and the system can thus be decoupled as shown in Fig. 5. The impedance $Z_{lk}$ for a capacitor (with a capacitance $C$) is $\frac{T}{C}$,
and for an inductor (with an inductance $L$) $L/T$, with $T$ being the simulation time step.

$$J_{CA}(k) = Y_C \cdot v_{CA}(k) = Y_C \cdot v_{CB}(k) + i_{CB}(k)$$  \hspace{1cm} (3)

Similarly for side B, we have

$$J_{CB}(k) = Y_C \cdot v_{CB}(k) = Y_C \cdot v_{CA}(k) + i_{CA}(k)$$  \hspace{1cm} (4)

For an inductor (DC choke) with an inductance $L$, the admittance of the TLM inductive link is $Y_L = T/L$. Applying the same procedure used above, we have

$$J_{LA}(k) = -Y_L \cdot v_{LB}(k) - i_{LB}(k)$$
$$J_{LB}(k) = -Y_L \cdot v_{LA}(k) - i_{LA}(k)$$  \hspace{1cm} (5)

C. The Taganrog Simulation/Hardware Interface

Fig. 8 shows the simulation/hardware interfacing scheme proposed by V. Popov et al. from the Taganrog State University of Radio Engineering, and it is referred to as the Taganrog simulation/hardware interface in this paper. Notice that current and voltage information on both sides are exchanged at each simulation time step. Also stabilizing factors $r_1$ and $r_2$ are inserted to ensure the stability of the decoupled simulation. The values of $r_1$ and $r_2$ can be chosen even when the system parameters are unknown.

D. The Simulation/Hardware Interface based on Time-Variant First-Order Estimation

The simulation/hardware interface based on time-variant first-order approximation (TFA) of the HUT is inspired by the idea of compensating the delay caused by the D/A, A/D conversion and elaboration time through approximating the dynamics of the HUT with a time-variant first-order system.

1) Inductive/Resistive HUT: If the HUT appears to be inductive or resistive at the main operation frequency, the dynamics of the real hardware system are approximated by the simulation/hardware interface as:

$$\frac{di_2}{dt} = a \cdot i_2 + b \cdot v_1$$  \hspace{1cm} (6)

Where $i_2$ is the current going into the HUT and $v_1$ the controlled voltage source applied across the HUT, whose value is determined by the output voltage of the ROS. Let us apply the trapezoidal integration method, and (6) can be discretized as follows:

$$i_2(k) = i_2(k-1) + \frac{a i_2(k) + b v_1(k) + a i_2(k-1) + b v_1(k-1)}{2} T_s$$  \hspace{1cm} (7)

Considering the ZOH effect of the voltage reference output by the ROS ($i.e., v_1(k) = v_1(k-1)$), (7) can be rearranged as:

$$i_2(k) = \alpha \cdot v_1(k-1) + \beta \cdot i_2(k-1) = G_{eq}(k) \cdot v_1(k) + I_{eq}(k)$$  \hspace{1cm} (8)
where \( \alpha = \frac{b \cdot T_s}{1 - a \cdot T_s} \) and \( \beta = \frac{1 + \frac{a \cdot T_s}{2}}{1 - \frac{a \cdot T_s}{2}} \). They can be solved as following:

\[
\begin{bmatrix}
\alpha \\
\beta
\end{bmatrix} =
\begin{bmatrix}
v_1 (k-1) & i_2 (k-1) \\
v_1 (k-2) & i_2 (k-2)
\end{bmatrix}^{-1}
\begin{bmatrix}
i_2 (k) \\
i_2 (k-1)
\end{bmatrix}
\tag{9}
\]

\[G_{\text{eq}}(k) = \alpha \]
\[I_{\text{eq}}(k) = \beta \cdot i_2 (k-1) \tag{10}\]

Fig. 9 shows the schematic of the TFA-based simulation/hardware interface for inductive/resistive HUT.

One problem with this interface is that solving (9) can raise numerical issues, especially when the system reaches steady state, and the matrix \( A = \begin{bmatrix} v_1 (k-1) & i_2 (k-1) \\ v_1 (k-2) & i_2 (k-2) \end{bmatrix} \) becomes singular. One solution is to keep the last previous estimation (i.e., \( I_{\text{eq}} \) and \( R_{\text{eq}} \) from the previous time step) when the system reaches steady state (i.e., the absolute value of the determinant of \( A \) is smaller than a certain limit). The estimation error caused by numerical issues is compensated for by adding a current source \( I_c \), as shown in Fig. 10.

The compensation current source \( I_c(k+1) \) can be calculated as follows:

\[I_C(k+1) = I_c(k) + K_i \cdot e(k) + e(k-1) \cdot Ts \tag{11}\]

where \( e(k) \) is the difference between the current of the ROS side and that of the HUT side, i.e., \( e(k) = i_1(k) - i_2(k) \). \( K_i \) is a constant, and should be chosen to be of the same magnitude as the reverse of the determinant of \( A \). The simulation results are not sensitive to the value of \( K_i \).

1) Capacitive/Resistive HUT: If the HUT appears to be capacitive or resistive at the main operation frequency, the dynamics of the real hardware system are approximated by the simulation/hardware interface as:

\[\frac{dv_2}{dt} = a \cdot i_1 + b \cdot v_2 \tag{12}\]

where \( v_2 \) is the voltage across the HUT, and \( i_1 \) the controlled current source going into the HUT, whose value is determined by the output current of the ROS. Let us apply the trapezoidal integration method, and (11) can be discretized as follows:

\[v_2(k) = v_2(k-1) + \frac{a_1 (k) + b v_2(k) + a_1 (k-1) + b v_2(k-1)}{2} \cdot T_s \tag{13}\]

Considering the ZOH effect of the voltage reference output by the ROS (i.e., \( i_1 = i(k-1) \)), (12) can be rearranged as:

\[v_2(k) = i_1(k-1) + v_2(k-1) = R_{\text{eq}}(k) \cdot i_1(k) + V_{\text{eq}}(k) \tag{14}\]

where \( \alpha = \frac{a \cdot T_s}{1 - b \cdot T_s} \) and \( \beta = \frac{1 + \frac{a \cdot T_s}{2}}{1 - \frac{a \cdot T_s}{2}} \). They can be solved as following:

\[
\begin{bmatrix}
\alpha \\
\beta
\end{bmatrix} =
\begin{bmatrix}
i_1 (k-1) & v_2 (k-1) \\
i_1 (k-2) & v_2 (k-2)
\end{bmatrix}^{-1}
\begin{bmatrix}
v_2 (k) \\
v_2 (k-1)
\end{bmatrix}
\tag{15}\]

In (14), \( R_{\text{eq}}(k) \) and \( V_{\text{eq}}(k) \) are equivalent resistance and voltage source, which approximate the time-variant HUT at time step \( k \). Their values are updated at each time step using current and voltage values at the previous time steps as follows:

\[R_{\text{eq}}(k) = \alpha \]
\[V_{\text{eq}}(k) = \beta \cdot v_2 (k-1) \tag{16}\]

As in the previous case, solving (20) can raise numerical issues here, especially when the system reaches steady state, and the matrix \( B = \begin{bmatrix} i_1 (k-1) & v_2 (k-1) \\ i_1 (k-2) & v_2 (k-2) \end{bmatrix} \) becomes singular. One solution is to keep the last previous estimation (i.e., \( V_{\text{eq}} \) and \( R_{\text{eq}} \) from the previous time step) when the system reaches steady state. The estimation error caused by numerical issues is compensated for by adding a voltage current source \( V_c \), as shown in Fig. 12.

The compensation current source \( V_c(k+1) \) can be calculated as follows:

\[V_C(k+1) = V_c(k) + K_v \cdot e(k) + e(k-1) \cdot Ts \tag{16}\]

where \( e(k) \) is the difference between the voltage across the ROS side and that across the HUT side, i.e., \( e(k) = V_1(k) - V_2(k) \). \( K_v \) is a constant, and should be chosen to be of the same magnitude as the reverse of the determinant of \( B \). The simulation results are not sensitive to the value of \( K_v \).
III. COMPARISON OF THE SIMULATION/HARDWARE INTERFACING SCHEMES

A. Decoupled Simulation of a First-Order System with an Inductive Load

The system under study is shown in Fig. 13. The parameters of this system are listed in Table 1. This system is partitioned into two subsystems—the voltage source and the inductive load—and different interfaces are inserted to simulate the PHIL experiment, as shown in Fig. 14. Since the TLM interfacing scheme actually replaces the DC choke inductor with the simulation/hardware interface, the decoupled system with the TLM interface has a different structure, as shown in Fig. 15.

![Fig. 13. The 1st-order system with the inductive load](image1)

**TABLE 1**

<table>
<thead>
<tr>
<th>Component</th>
<th>Variable</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>voltage source E (E(t)=Acos(2πft))</td>
<td>amplitude (A)</td>
<td>100V</td>
</tr>
<tr>
<td></td>
<td>frequency (f)</td>
<td>50Hz</td>
</tr>
<tr>
<td></td>
<td>resistance (R)</td>
<td>1Ω</td>
</tr>
<tr>
<td>load</td>
<td>resistance (R)</td>
<td>5Ω</td>
</tr>
<tr>
<td></td>
<td>inductance (L)</td>
<td>1mH</td>
</tr>
</tbody>
</table>

![Fig. 14. The decoupled system with the simulation/hardware interface](image2)

![Fig. 15. The decoupled system with the simulation/hardware interface](image3)

![Fig. 16. The IHUT waveforms (configuration 1)](image4)

**TABLE 2**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>IROS</td>
<td>Current through the ROS side of the system</td>
</tr>
<tr>
<td>VROS</td>
<td>Output voltage across the ROS side of the system</td>
</tr>
<tr>
<td>VHUT</td>
<td>Voltage across the HUT side of the system</td>
</tr>
<tr>
<td>I_org</td>
<td>Current through the original system</td>
</tr>
<tr>
<td>IROS_itm</td>
<td>I ROS in the system with the ITM-based interface</td>
</tr>
<tr>
<td>IROS_tg</td>
<td>I ROS in the system with the Taganrog interface</td>
</tr>
<tr>
<td>IROS_tlm</td>
<td>I ROS in the system with the TLM-based interface</td>
</tr>
<tr>
<td>IROS_tfa</td>
<td>I ROS in the system with the TFA-based interface</td>
</tr>
<tr>
<td>IHUT_itm</td>
<td>I HUT in the system with the ITM-based interface</td>
</tr>
<tr>
<td>IHUT_tg</td>
<td>I HUT in the system with the Taganrog interface</td>
</tr>
<tr>
<td>IHUT_tlm</td>
<td>I HUT in the system with the TLM-based interface</td>
</tr>
<tr>
<td>IHUT_tfa</td>
<td>I HUT in the system with the TFA-based interface</td>
</tr>
<tr>
<td>VROS_org</td>
<td>V ROS in the original system</td>
</tr>
<tr>
<td>VROS_itm</td>
<td>V ROS in the system with the ITM-based interface</td>
</tr>
<tr>
<td>VROS_tg</td>
<td>V ROS in the system with the Taganrog interface</td>
</tr>
<tr>
<td>VROS_tlm</td>
<td>V ROS in the system with the TLM-based interface</td>
</tr>
<tr>
<td>VROS_tfa</td>
<td>V ROS in the system with the TFA-based interface</td>
</tr>
</tbody>
</table>

Fig. 16 shows the simulation results with a simulation time step of 10μs. The meaning of the symbols in the graphs is listed in Table 2. The stabilizing factors in the Taganrog interface are chosen as: \( r_1=r_2=r=100\Omega \). It can be seen from Fig. 16 that all the decoupled systems yield simulation results close to those of the original system. To compare the performance of these interfacing schemes, a relative error

\[
\varepsilon_r = \frac{\|e\|_2}{\|x\|_2}
\]

is introduced, where \( \|e\|_2 \) is the second norm of the error, and \( \|x\|_2 \) is the second norm of the state under analysis. For example, the relative error of the voltage across the ROS is

\[
\varepsilon_r - V_{ROS} = \frac{\|e - V_{ROS}\|_2}{\|V_{ROS \_org}\|_2}.
\]

A comparison of the relative errors of different interfaces is made in Table 3.
It can be seen that the system with the TLM-based interface gives the biggest relative error in $I_{\text{ROS}}$, while the system with the biggest relative error in $V_{\text{HUT}}$ is the one with the ITM-based interface. The decoupled system with the TFA-based interface yields the closest results to those of the original system overall. Furthermore, it is also found that for the system with the Taganrog interface, the value of the stabilizing factor $r_1$ and $r_2$ have an impact on the simulation results. For the results shown in Fig. 16, $r_1$ and $r_2$ are chosen as: $r_1=r_2=100\Omega$. If decrease the values of $r_1$ and $r_2$ to 1\Omega, the steady state error yielded by the system with the Taganrog interface increases, as can be seen in Table 3 and Fig. 17.

<table>
<thead>
<tr>
<th>Interface</th>
<th>$e_{I_{\text{ROS}}}$</th>
<th>$e_{V_{\text{HUT}}}$</th>
<th>$e_{V_{\text{HUT}}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>ITM</td>
<td>6.200e-3</td>
<td>3.000e-3</td>
<td>1.207e-4</td>
</tr>
<tr>
<td>Taganrog</td>
<td>4.500e-3</td>
<td>6.100e-3</td>
<td>8.748e-5</td>
</tr>
<tr>
<td>TLM</td>
<td>5.000e-3</td>
<td>9.800e-3</td>
<td>9.756e-5</td>
</tr>
<tr>
<td>TFA</td>
<td>4.100e-3</td>
<td>3.100e-3</td>
<td>8.042e-5</td>
</tr>
</tbody>
</table>

**TABLE 3**
RELATIVE ERROR IN THE SIMULATION RESULTS FROM DIFFERENT INTERFACES (SYSTEM CONFIGURATION 1)

In the previous case, the input voltage source $E$ is a sinusoidal signal with zero phase angle (*i.e.*, $E(t=0) = 0V$). To study the transient response of the decoupled system, $E$ is changed to a cosine signal, *i.e.*, $E(t=0) = 100V$. Also to study the how the different interfaces react to the dynamic change of the HUT, the resistance of the load $R_2$ is started at 51\Omega, and then changed to 1\Omega at $t = 50ms$. The configuration of the system is listed in Table 4, and the simulation results of the decoupled systems are shown in Fig. 18.

It can be seen from Fig. 18 the decoupled system with the TLM interface has a longer transient and bigger oscillation than the others when the load changes. The other decoupled systems have rather smooth transitions. This can be better demonstrated through Fig. 19.

**TABLE 4**
PARAMETERS OF THE 1<sup>st</sup>-ORDER SYSTEM WITH THE INDUCTIVE LOAD – CONFIGURATION 2

<table>
<thead>
<tr>
<th>Component</th>
<th>Variable</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>voltage source $E$</td>
<td>amplitude (A)</td>
<td>100V</td>
</tr>
<tr>
<td>frequency (f)</td>
<td>50Hz</td>
<td></td>
</tr>
<tr>
<td>resistance ($R_c$)</td>
<td>1\Omega</td>
<td></td>
</tr>
<tr>
<td>load</td>
<td>resistance ($R_c$)</td>
<td>51\Omega \rightarrow 1\Omega</td>
</tr>
<tr>
<td></td>
<td>inductance (L)</td>
<td>1mH</td>
</tr>
</tbody>
</table>

**B. Decoupled Simulation of a First-Order System with a Capacitive Load**

The system under study is shown in Fig. 20. The parameters of this system are listed in Table 6. This system is partitioned into two subsystems: the voltage source and the capacitive load. Different interfaces are then inserted to simulate the PHIL experiment, as shown in Fig. 21. Since the TLM interfacing scheme actually replaces the DC voltage smoothing capacitor with the simulation/hardware interface, the decoupled system with the TLM interface has a different structure, as shown in Fig. 22.

![Fig. 20. The 1<sup>st</sup>-order system with the capacitive load](image)
To study how the different interfaces react to the dynamic change of the HUT, the resistance of the load $R_2$ is started at 51 Ω, and then changed to 1 Ω at $t = 50$ ms. The configuration of the system is listed in Table 6, and the simulation results of the decoupled systems are shown in Fig. 23.

### TABLE 6
<table>
<thead>
<tr>
<th>Component</th>
<th>Variable</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>voltage source E</td>
<td>amplitude (A)</td>
<td>100V</td>
</tr>
<tr>
<td></td>
<td>frequency (f)</td>
<td>50Hz</td>
</tr>
<tr>
<td></td>
<td>resistance (R_e)</td>
<td>1Ω</td>
</tr>
<tr>
<td>load</td>
<td>resistance (R_e)</td>
<td>51Ω→1Ω</td>
</tr>
<tr>
<td></td>
<td>capacitance (C)</td>
<td>1mF</td>
</tr>
</tbody>
</table>

As can be seen from Fig. 23, the system with the Taganrog interface has a longer transient and larger oscillation than the other decoupled systems. As in the previous two cases, the decoupled systems with the ITM-, the TLM-, and the TFA-based interface yield results close to those of the original system while the system with the Taganrog interface gives a bigger steady state error than others.

### IV. CONCLUSIONS

In this paper, different simulation/hardware interfacing schemes for PHIL experiments are introduced, and their performance compared through the decoupled simulation of the first-order systems. The ITM- and the TFA-based interfaces give the best overall performance in terms of steady state error, sensitivity to the initial conditions, and the response to the dynamics of the HUT. Relative error is introduced as a criterion to determine the performance of the PHIL simulations. However, the relative error is not able to provide the designer with the information about the transient response of the PHIL systems. Therefore, a more advanced analysis process based on wavelet transforms will be introduced in Part II.

### V. ACKNOWLEDGMENT

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### VI. REFERENCES


